VISIT Deliverable Report Cover Sheet

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Deliverable description and summary of achieved results (max. 2400 char.):

This report is the second part of two stages in the description of the system specifications surrounding the VCSEL based high speed optical link.

The report is structured as follows:

Section 1 investigates the impact of high speed 40Gb/s VCSEL sources on the driver requirments. The methodology behind the design of a CMOS driver suitable for DM VCSELs developed within VISIT is shown. A complete VERILOG-A VCSEL model is obtained based on intrinsic and extrinsic parameters directly measured on DM VCSELs from VISIT. The feasibility of 65nm CMOS for the 40Gb/s VCSEL driver is also demonstrated. Advanced design features include adjustable pre- and de-emphasis and input equalization to optimize the optical eye and compensate for expected variations of VCSEL performance. Finally, different options for the driver circuitry environment are discussed.

Section 2 is a theoretical investigation of the suitability of multilevel signaling schemes for high speed 850nm transmission over OM3 fibers. The main trade-offs and link performance are provided in order to compare multilevel schemes with faster NRZ transceivers. Further, achievable receiver sensitivity at 850 nm wavelength range is discussed for high-speed links.

Finally, Section 3 discusses the suitability of VISIT DM VCSELs for analog links such as 802.11g wireless LAN constellations. This discussion is based on some of the outcome experimental results from WP4.

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Table of Contents

List of Figures

1. VCSEL driver specification and design

1.1. Introduction

This section describes the specification and feasibility of a 40Gb/s VCSEL driver, intended for direct NRZ modulation of VCSELs. One can distinguish between two approaches for such a VCSEL driver:

1. Design of a 'generic' VCSEL driver, meaning that it is designed in such a way as to support a large range of VCSEL parameters such as threshold current, slope efficiency etc. The drawback of this approach is that it leads to a larger (in terms of die area), more complicated driver design.
2. Design of a 'specific' VCSEL driver, intended for a VCSEL with well defined parameters such as threshold current, slope efficiency etc. While this allows simplification of the driver design, the obvious drawback is that the driver doesn't work for VCSELs which are significantly different from the targeted VCSEL.

Here, it was chosen to design a generic VCSEL driver. The main reasons for this choice are:

1. The high-speed VCSEL devices are still experimental devices, whose successive generations may exhibit widely varying parameters,
2. Once such a generic VCSEL driver has been designed and tested successfully, the design of a more specific VCSEL driver is a straightforward exercise.

Furthermore, for this first version of the VCSEL driver, the main focus is to ensure proper operation of the high-speed data path. Therefore, no automatic power control circuitry will be included on-chip. Rather, the bias and modulation currents will be fully programmable using a serial digital interface. This would allow the construction of an automatic power control loop using external off-the-shelf components should this be required.

1.2. Results of VCSEL modelling for driver design

Design of a VCSEL driver at frequencies above 10GHz requires a detailed model of the VCSEL that can be co-simulated with the transistor level circuits of the driver itself. Such a model must accurately capture both the electrical impedance of the VCSEL (electrical parasitics) over a broad frequency range as well as its electro-optical response. Here, it was chosen to implement a simplified model of the electro-optical response based on single-mode rate equations. While more advanced (and accurate) models can be built, in general these require very long simulation times and exhibit simulator convergence problems, and were therefore found to be less useful for the intended verification of the transistor level design of the VCSEL driver.

1.2.1. VCSEL rate equations

The VCSEL rate equations used are:

$$\begin{aligned}\frac{dN}{dt} &= \frac{h_i I}{qN_w V_{ACT}} - R(N) - \Gamma v_{gr} G(N,S) S \\ \frac{dS}{dt} &= N_w R_b(N) + N_w \Gamma v_{gr} G(N,S) S - \frac{S}{t_P}\end{aligned} \quad (1)$$

with N the carrier density, I the driving current and S the normalized photon density S = S_{TOT}/V_{act}, S_{TOT} being the photon number [1]. The various parameters are listed in Table 1.

Table 1 – Rate equation parameters.

Symbol	Description	Unit
η_i	Internal current efficiency	-
N_w	Number of quantum wells	
V_{act}	Volume of a single quantum well	m^3
R(N)	Carrier recombination rate	s^{-1}
G(N,S)	Gain function	-
g_0	Gain slope	m^{-1}
Γ	Carrier confinement factor	-
v_{gr}	Velocity of light in the cavity	m/s
ε	Gain saturation parameter	m^3
$R_\beta(N)$	Coupled spontaneous emission	s^{-1}
β	Spontaneous emission factor	-
τ_n	Carrier lifetime	S
τ_p	Photon lifetime	s
λ	Emission wavelength	m

The gain function G(N,S) is assumed to have the following form:

$$G(N,S) = \frac{g_0}{N_0} \frac{N(t) - N_0}{1 + e\Gamma S(t)} \quad (2)$$

with ε the gain saturation parameter and N_0 the carrier density at transparency. The carrier recombination rate is modelled as:

$$R(N) = \frac{N(t)}{t_n} \quad (3)$$

with τ_n the carrier lifetime. Finally, the coupled spontaneous emission is modelled as:

$$R_b(N) = b \frac{N(t)}{t_n} \quad (4)$$

with β the spontaneous emission factor. The VCSEL output power can be derived from the photon density using:

$$P(t) = \frac{Vh_i hc}{2\Gamma t_p l} S(t). \tag{5}$$

1.2.2. Parameter extraction for rate equations

The parameters for the rate equation model can be extracted using the following procedure. First the rate equations are transformed to the following form [2]:

$$\begin{aligned} \frac{dP}{dt} &= \frac{Bt_n I_{th}(X(t)-1)+\frac{1}{t_p}}{1+fBt_p t_c P(t)} P(t) - \frac{P(t)}{t_p} + \frac{I_s I_{th} Bt_n}{f} X(t) \\ \frac{dX}{dt} &= \frac{I(t)}{I_{th} t_n} - \frac{fBt_p(X(t)-1)+\frac{f}{I_{th} t_n}}{1+fBt_p t_c P(t)} P(t) - \frac{X(t)}{t_n} \end{aligned} \tag{6}$$

where X(t) is the relative carrier density:

$$X(t) = \frac{N(t)}{N_{th}} \tag{7}$$

with N_{th} the carrier density that corresponds to the condition where cavity losses and cavity gain exactly balance each other:

$$\Gamma v_{gr} \frac{g_0}{N_0} \frac{N_{th} - N_0}{1+e\Gamma S} = \frac{1}{t_p}. \tag{8}$$

I_{th} is the threshold current density:

$$I_{th} = \frac{qN_w V_{act} N_{th}}{t_n} \tag{9}$$

and I_s is the spontaneous emission current:

$$I_s = \frac{b}{Bt_n t_p}. \tag{10}$$

B and τ_c are given by:

$$B = \frac{\Gamma v_{gr}}{qN_w V_{act}}; \qquad t_c = \frac{e}{v_{gr}}. \tag{11}$$

The rate equations are now completely defined by seven parameters I_{th}, I_s, B, τ_n, τ_p, τ_c and ϕ. I_{th}, I_s and ϕ can be extracted from the dc-characteristics, which can be obtained from (6) by setting the derivatives equal to zero:

$$(f\,P)^2 - (I - I_{th} - I_s) f\,P - I_s I = 0. \tag{12}$$

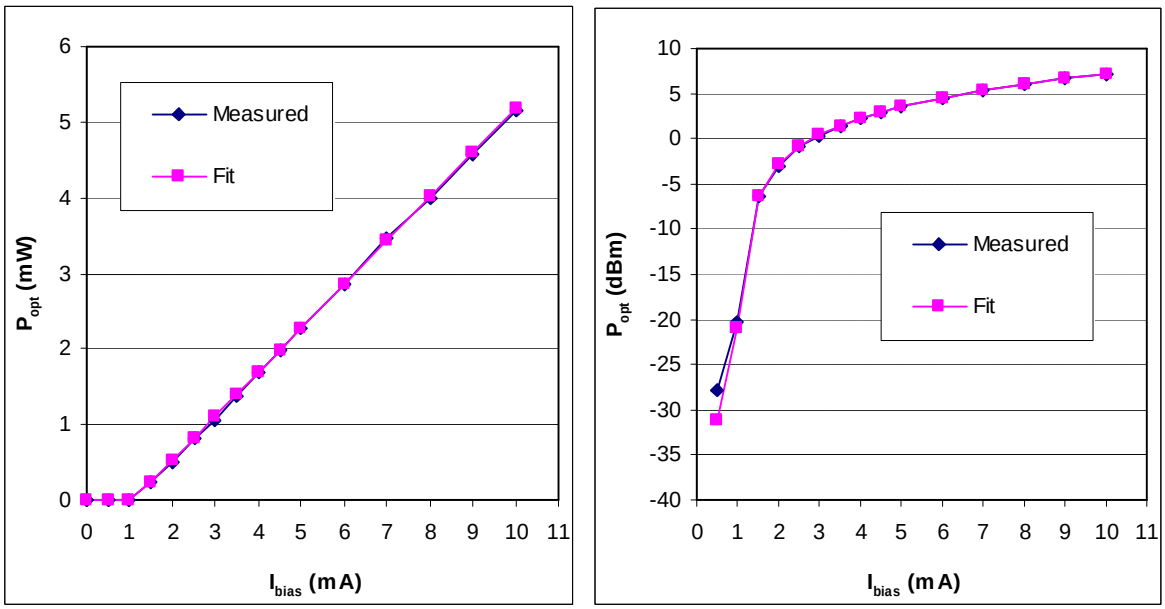


Figure 1 – Measured and fitted (L,I) curves.

An example of such a fitting is shown in Figure 1. The extracted values are given in Table 2.

Table 2 – Extracted parameters from (L,I) curves.

Parameter	Extracted value	Unit
I_s	1.62	µA
I_{th}	1.1	mA
ϕ	1.72	A/W

The other parameters can be extracted using a frequency subtraction method [3]. This method consists of modulating the VCSEL bias with a small signal and measuring the corresponding frequency response using a photodetector. The intrinsic VCSEL frequency response (i.e. the response obtained if the laser would not exhibit any electrical parasitics) can be shown to have a second-order behaviour determined by a relaxation oscillation frequency f_r and a damping rate Γ_d:

$$|H(f)|^2 = \frac{f_r^4}{\left(f^2 - f_r^2\right)^2 + \left(\frac{\Gamma_d}{2p}\right)^2 f^2}. \qquad (13)$$

While in principle one can directly measure H(f) (as a function of VCSEL bias current) using e.g. a network analyzer, a major problem is the fact that the bandwidth limitations (incurred by the laser parasitics and the photodetector response) reduce the accuracy of this measurement due to limitations in dynamic range of the vector network analyzer. An elegant solution consists of measuring the frequency response for a range of different bias currents. This range should start just above the threshold current of the VCSEL up to some upper boundary over which the VCSEL model should operate correctly. Then, the lowest bias frequency response is subtracted from the other responses. The thus obtained frequency response H'(f) (see (14)) is determined solely by the intrinsic laser response, as indeed the photodetector response and VCSEL parasitics are independent from the VCSEL bias current.

$$|H'(f)|^2 = \frac{f_{r1}^4}{\left(f^2 - f_{r1}^2\right)^2 + \left(\frac{\Gamma_{d1}}{2p}\right)^2 f^2} \frac{\left(f^2 - f_{r0}^2\right)^2 + \left(\frac{\Gamma_{d0}}{2p}\right)^2 f^2}{f_{r0}^4}. \qquad (14)$$

By fitting a number of frequency responses to (14) the resonance frequency and damping factor can be extracted as a function of bias current. The frequency responses can be measured using the setup in Figure 2.

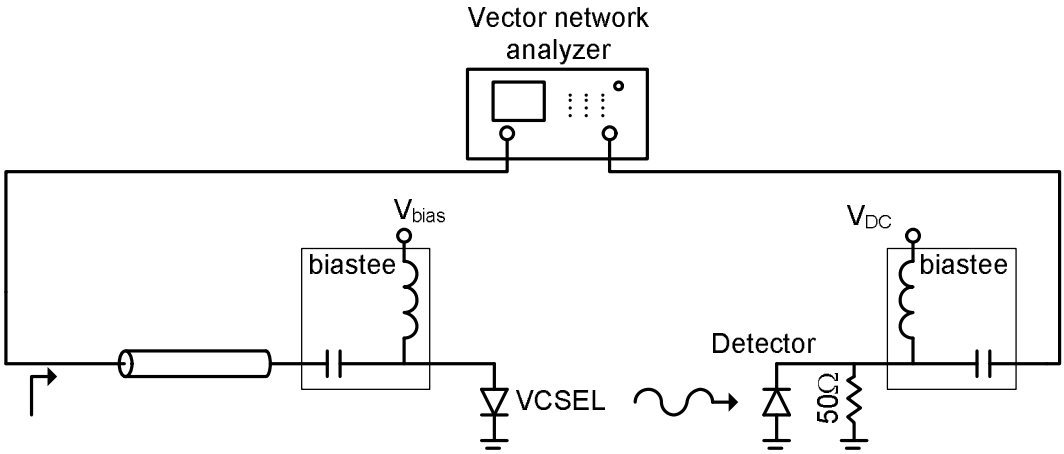


Figure 2 – Measurement setup for measuring the VCSEL frequency response.

It can be shown that the relaxation oscillation frequency fr is related to the VCSEL bias current by (for sufficiently small bias currents):

$$f_r = \frac{\sqrt{B(I_{bias} - I_{th})}}{2p}. \quad (15)$$

From (15) one can extract the parameter B. Next, it can be shown that the damping rate Γ_d is given by:

$$\Gamma_d = \frac{1}{t_n} + Kf_r^2. \quad (16)$$

with K the so-called universal K-factor:

$$K = 4p^2(t_p + t_c). \quad (17)$$

By plotting Γ_d as a function of I_{bias} we can extract K and τ_n. Finally, by assuming a value for the photon lifetime from e.g. literature, τ_c can be extracted using (17).

1.2.3. VCSEL electrical parasitics and equivalent model

Figure 3 shows a simplified model of the electrical parasitics. C_{BP} is the parasitic capacitance stemming from the VCSEL bondpad structure. R_S is the active region series resistance and C_J is the capacitance of the forward biased junction. R_{act} is the differential resistance of the active region.

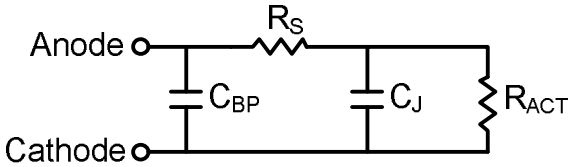


Figure 3 – VCSEL parasitics.

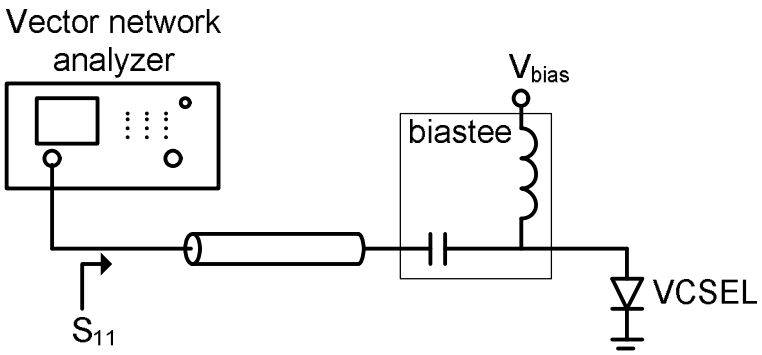


Figure 4 – Measurement setup for measuring the VCSEL parasitics.

These parameters can be extracted by measuring S_{11} using a vector network analyzer (see setup in Figure 4), and fitting them to the described model. Figure 5 shows an example of such a fit for a tested VCSEL sample (Ibias = 10mA), Figure 6 gives the extracted values for one of the tested VCSELs.

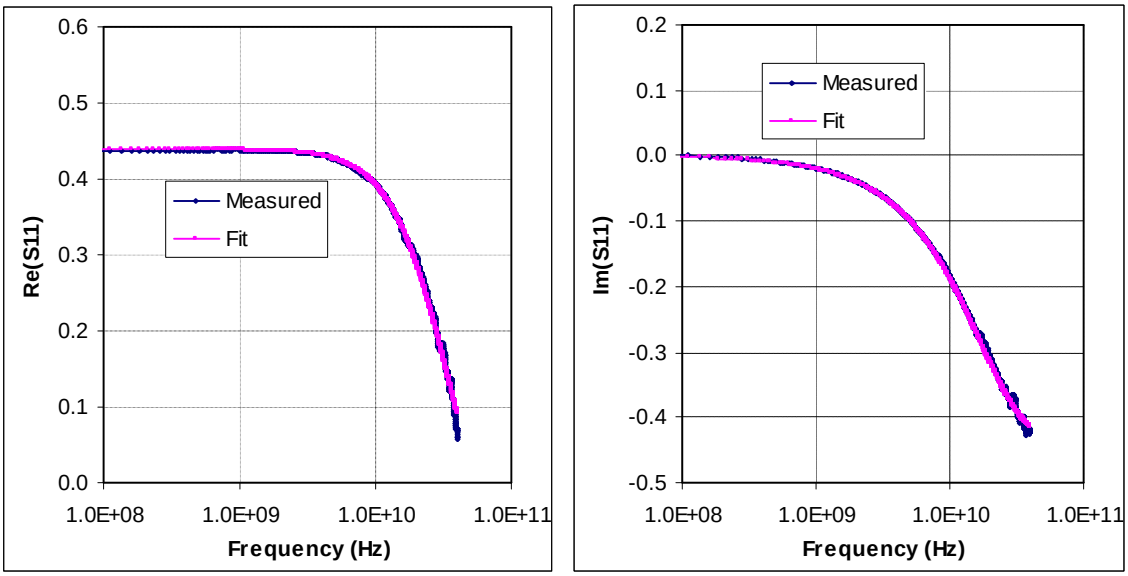


Figure 5 – S_{11} fit (I_{bias} = 10mA) – real and imaginary parts.

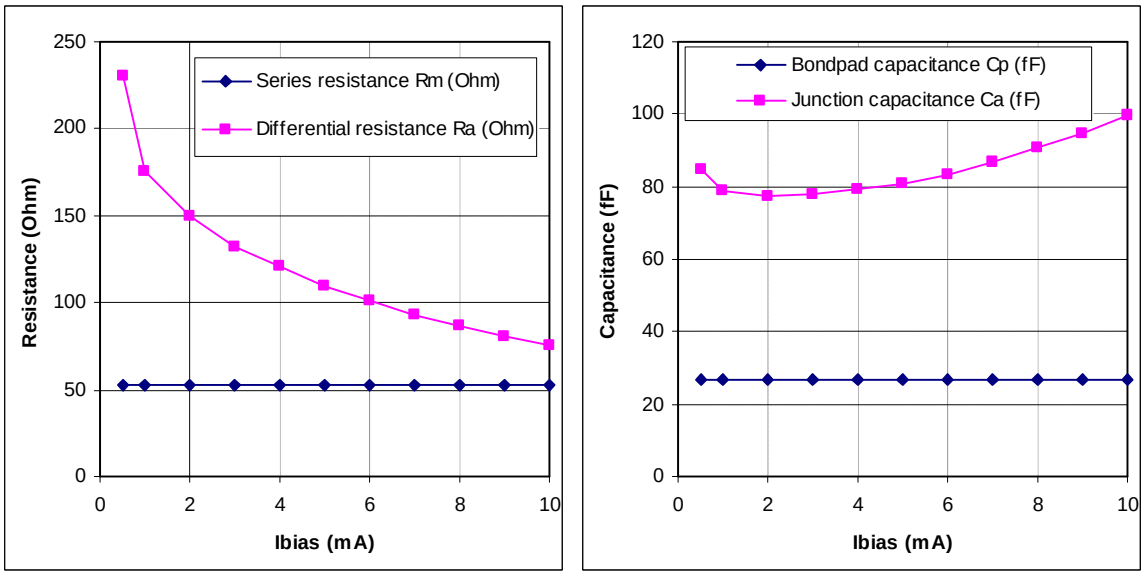


Figure 6 – Fitted parasitics vs. bias current.

As will be pointed out later, a more detailed model of the parasitics might be required. Such a model can be obtained with the aid of electromagnetic modelling software, see Figure 7. In a first step, the 'full-field' S-parameters are extracted using the electromagnetic modelling software. Next, a lumped equivalent circuit (see Figure 8) is constructed. Using a quasi Newton fitting procedure, the values of the lumped components are fitted such that the S-parameters of the equivalent lumped circuit equal the 'full-field' S-Parameters. The fitted

component values are listed in Table 3. Figure 9 to Figure 11 shows how the model captures the essential behaviour of the parasitics over a wide frequency range.

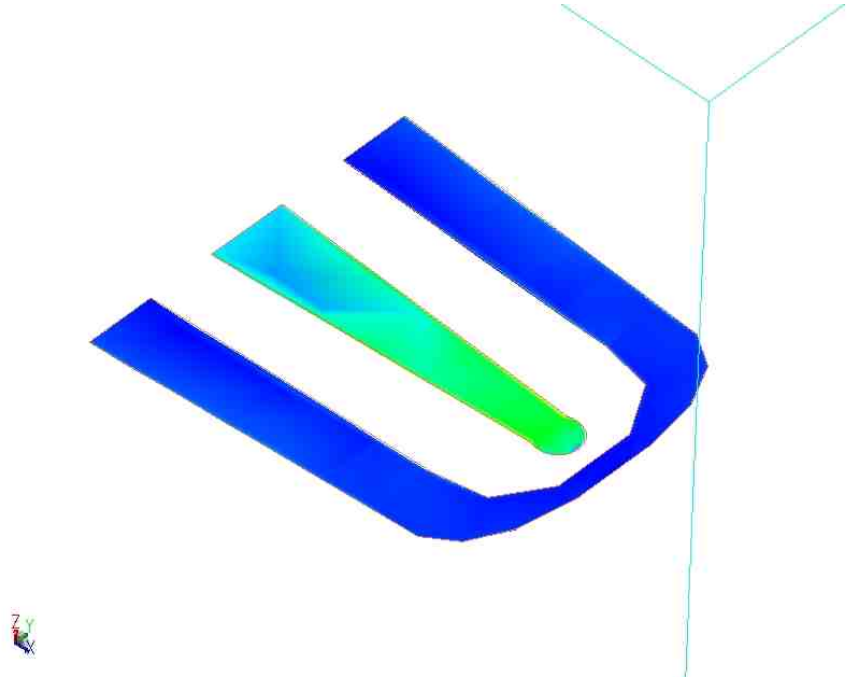


Figure 7 – Electromagnetic simulation showing surface current density of interconnection structure on the VCSEL (f=40GHz).

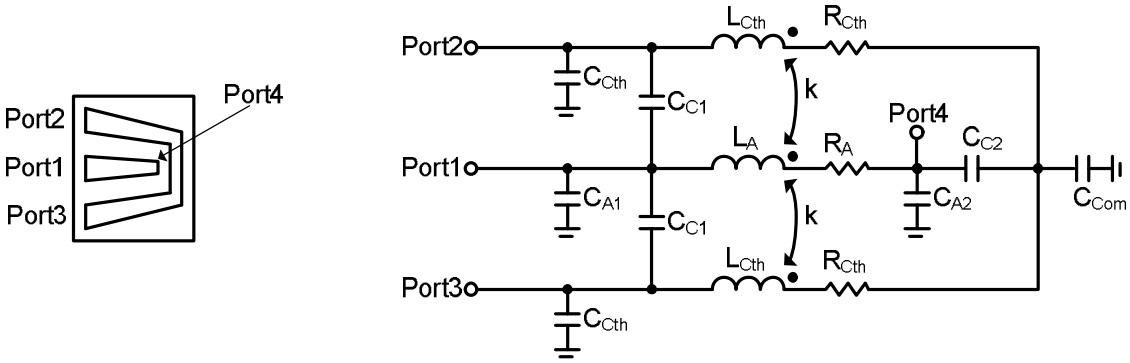


Figure 8 – Equivalent lumped model of the VCSEL interconnection parasitics.

Table 3 – Fitted values for the equivalent lumped model.

Parameter	Extracted value	Unit
C_{A1}	16.6	fF
C_{A2}	6.9	fF
C_{Cth}	21.7	fF
C_{c1}	2.3	fF
C_{c2}	20.0	fF
C_{com}	36.6	fF
k	0.38	-
L_A	187	pH
L_{Cth}	255	pH
R_A	0.07	Ω
R_{Cth}	0.73	Ω

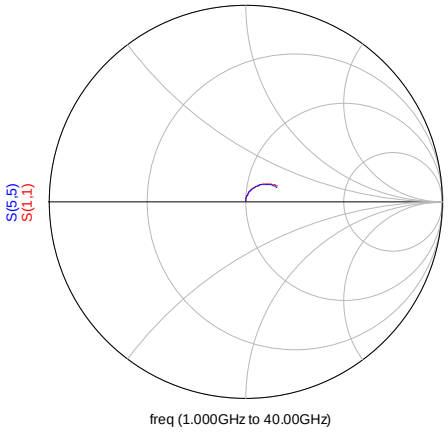


Figure 9 – S11 (red=fit, blue=full-field simulation).

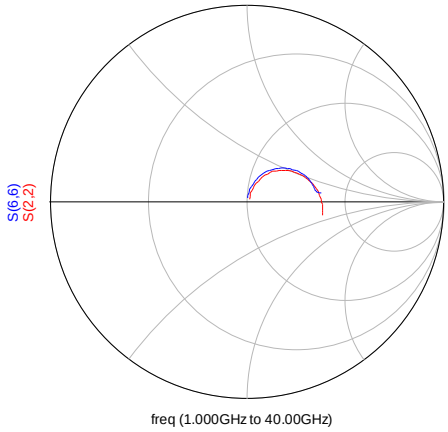


Figure 10 – S22 (red=fit, blue=full-field simulation).

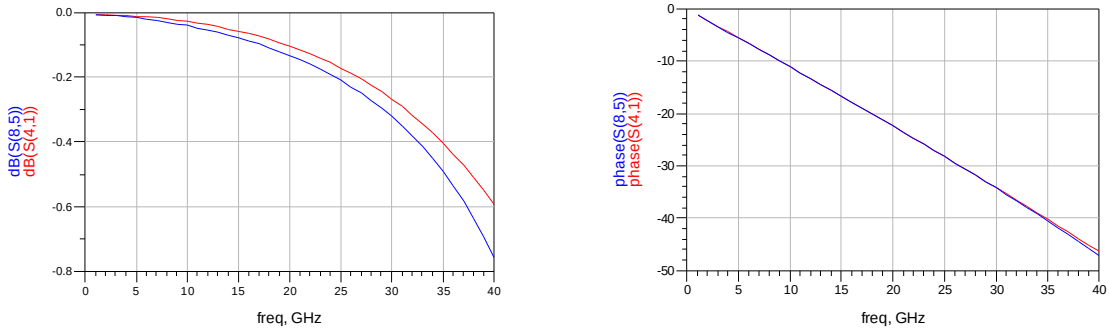


Figure 11 – Magnitude and phase of S41 (red=fit, blue=full-field simulation).

1.2.4. Complete VCSEL model based on Verilog-A

Figure 12 shows the final VCSEL model, which is fully compatible with transistor-level circuit simulators. The parasitics have been implemented using standard components, the transformed rate equations (6) have been implemented using Verilog-A. The driving current for the Verilog-A model is the current through the active region differential resistance. In the Verilog-A model, both the normalized electron density and the VCSEL optical output power are represented as voltages. It is to be noted that the transformed VCSEL rate equations offer a significant advantage when implemented in a Verilog-A model. Indeed the actual numbers representing the optical output power and normalized electron density are similar to the numerical values of voltages encountered in typical CMOS circuits. This is contrary to the 'standard' formulation of the rate equations in terms of photon and electron densities, whose numerical values range between 10^{15} and 10^{30}. Circuit simulators may exhibit convergence problems when having to handle such numbers. Table 4 lists the parameters used in the VCSEL model.

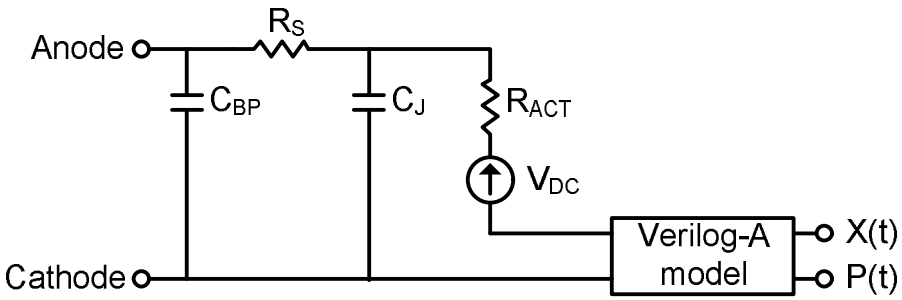


Figure 12 – Complete VCSEL model.

If so required, the more detailed interconnection parasitics as discussed previously may be added to the model.

Table 4 –Parameters for the VCSEL model.

Parameter	Extracted value	Unit
I_s	1.62	µA
I_{th}	1.10	mA
ϕ	1.72	A/W
τ_n	0.3	ns
τ_p	3.3	ps
τ_c	3.9	ps
B	1770	GHz^2/mA

Figure 13 and Figure 14 show several results using the constructed model. First the (L,I) curve is simulated; close correspondence with the curve in Figure 1 can be observed. Next, an eye diagram at 30Gb/s is generated, the bias current was 4mA and the modulation current was 10mA.

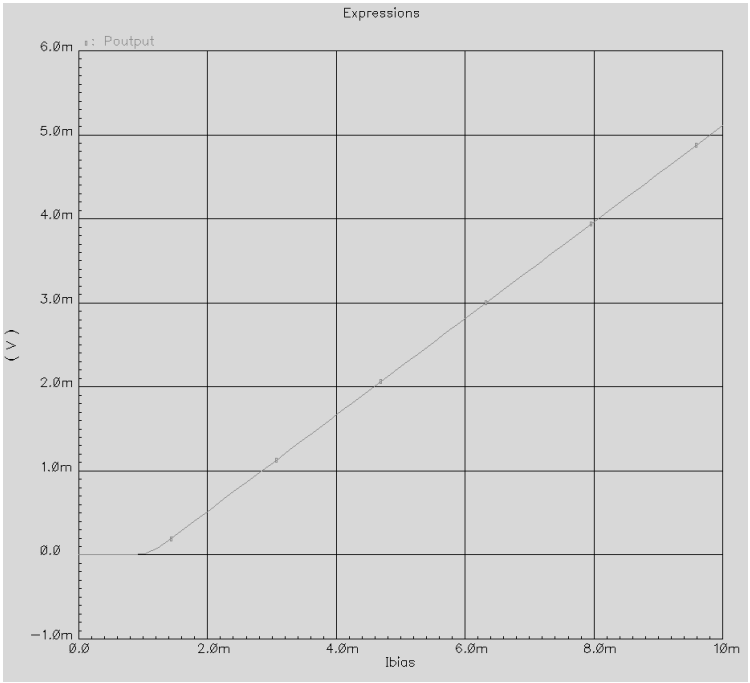


Figure 13 – (L,I) curve from VCSEL model simulated with Cadence Spectre.

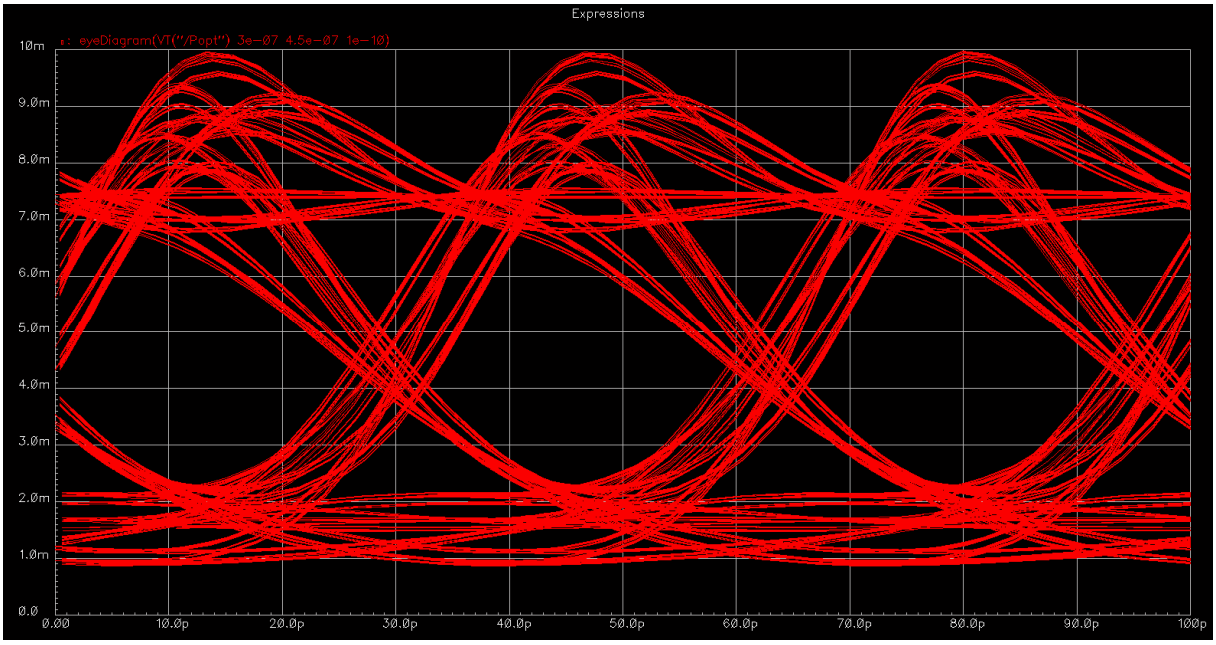


Figure 14 – 30Gb/s eye from VCSEL model simulated with Cadence Spectre.

1.3. VCSEL driver specification

1.3.1. Functionality and block diagram of the VCSEL driver

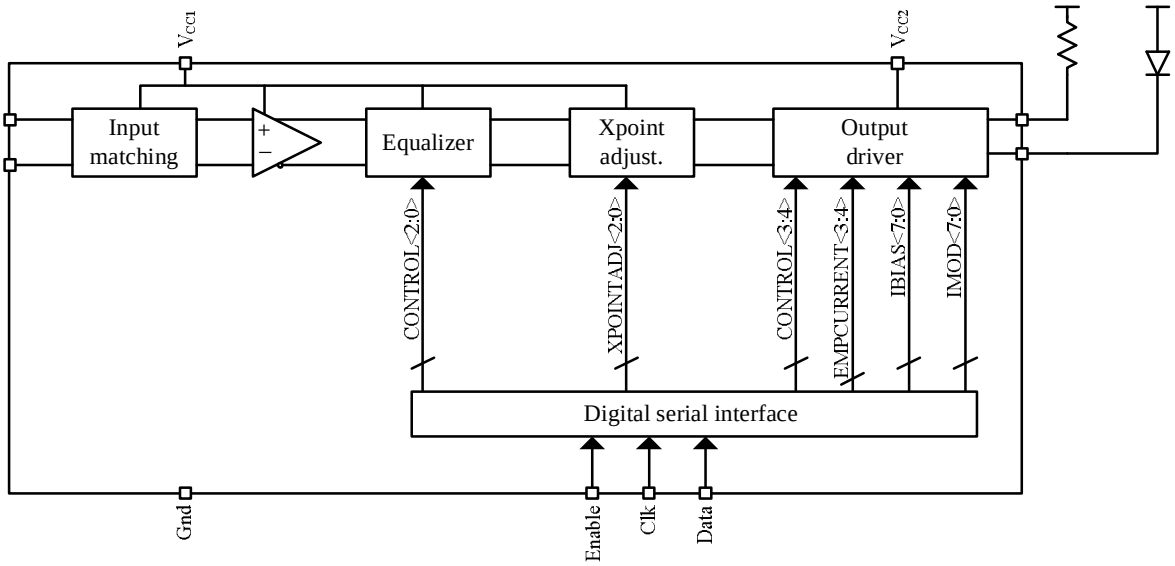


Figure 15 – Functional block diagram of the VCSEL driver.

The VCSEL driver is designed for 40Gb/s direct modulation of bare chip VCSELs with a differential resistance ranging from 50Ω to 100Ω. It is specifically designed to be integrated together with a VCSEL into a TOSA (transmitter optical subassembly) package. Note that this differs from more conventional solutions whereby a laser diode is assembled into a TOSA package and the laser driver is external to the TOSA package. The view taken here is that the

electrical interconnection between the VCSEL and driver circuit is highly critical, and performance (signal integrity) will be better if the interconnection between the VCSEL and output driver can be kept as short as possible.

The driver accepts a 40Gb/s NRZ current-mode logic differential input signal. An on-chip matching network ensures good input return loss up to 40GHz. An adjustable equalizer compensates for the insertion loss of packaging and transmission line traces.

The output modulation waveform is adjustable by programming a series of digital-to-analogue converters (DAC), each programmable through a serial digital interface. Individually adjustable rising and falling edge, pre- or de-emphasis is provided to maximize the optical eye opening. Further optimization of the eye opening is provided by modulation crossing point adjustment. This first version of the chip does not include automatic power control. The output electrical waveform can be fully digitally controlled. Figure 15 shows a functional block diagram of the VCSEL driver.

1.3.2. Selection of suitable silicon technology

Two technologies were considered for designing the VCSEL driver:

- 65nm CMOS technology
- 40nm CMOS technology

Preliminary simulations clearly showed that the design kit and models which are currently licensed on the market for 40nm CMOS technology were not yet fully mature. As this is a risk for the design, the 65nm CMOS technology was selected. Figure 16 finally shows that it is possible to achieve sufficiently fast switching speeds for 40Gb/s operation. Shown is a differential pair switching a 15mA current through 50Ohm resistive loads, resulting in a 750mV single-ended voltage swing. Rise and fall times are in the range of 5ps.

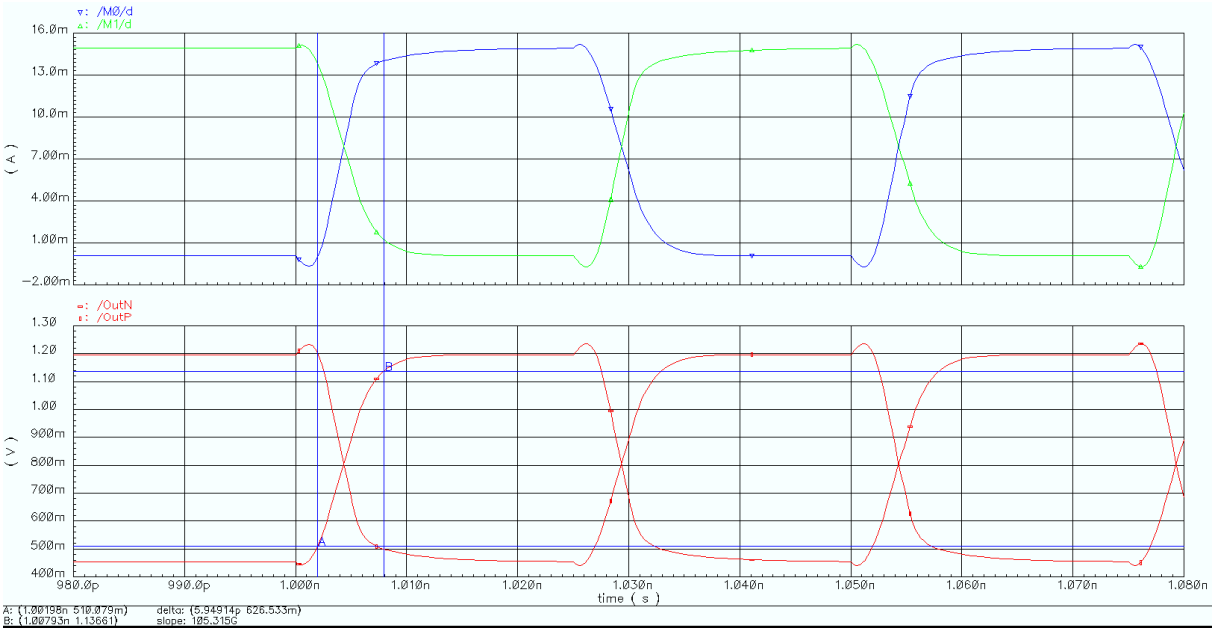


Figure 16 – Simulation of switching speed in 65nm CMOS (upper traces: currents, lower traces: voltages).

1.3.3. Environmental specification

Table 5 – Environmental specifications.

Parameter	Min.	Typ.	Max.	Unit	Remarks
Operating temperature range	0	27	85	°C	
Core supply voltage	1.08	1.20	1.32	V	+/-10%
Output driver supply voltage	1.62	1.80	1.98	V	+/-10%

Table 5 gives the environmental specification. Two different power supplies will be used:

1. The 1.2V domain: input structures, input equalizer and crosspoint adjustment and output driver
2. The 1.8V domain: pre-driver and biasing

The reason for splitting up the power supplies in this way are:

1. The 1.2V domain is used for the high-speed switching transistors
2. Some parts of the circuit such as IO transistors (which have thicker oxides) and biasing may require a 1.8V supply voltage

The currently specified +/- 10% tolerance on the supply voltages may be too challenging for certain parts of the driver circuit. If this is the case, this specification will be relaxed towards +/- 5%.

1.3.4. Specification of electrical input

Table 6 gives the specifications for the differential electrical input. Compared to more conventional (e.g. current-mode logic) signalling formats, the differential swing has been reduced due to the low input supply voltage (1.2V). The driver expects an ac-coupled input.

Table 6 – Differential input of the driver.

Parameter	Min.	Typ.	Max.	Unit	Remarks
Differential swing	300		500	mV	
Input common-mode voltage	0.7	0.8	0.9	V	+/-10%

The input to the driver chip is differential, which offers high immunity to electromagnetic interference (which can be considered to be common-mode with respect to the inputs). Furthermore, from the viewpoint of the circuit design, the self-referencing nature of differential signalling allows to achieve significantly improved distortion characteristics compared to a single-ended input. High immunity to common-mode interference requires that the differential signal lines must be physically as close as possible. Further, given the high bandwidth (~40GHz) transmission lines must be used to connect to the inputs of the driver. Hence, the transmission lines needed to connect to the inputs of the driver must be coupled transmission lines. It is important to specify the input return loss accordingly. Hence, rather than specifying single-ended return loss, the differential mode return loss (S_{DD11}), differential-to-common-mode conversion (S_{CD11}) and common-mode input return loss (S_{CC11}) are specified here [4]. Figure 17 shows how the driver circuit can be modelled as a four-port in terms of conventional S-parameters.

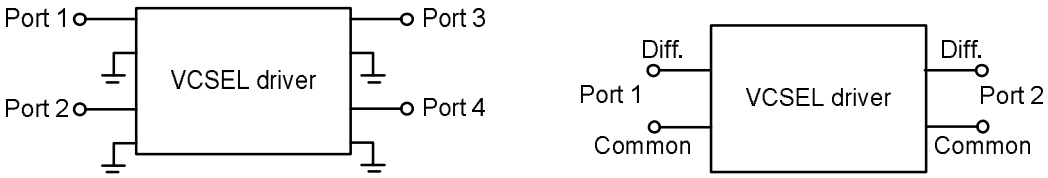


Figure 17 – Mixed-mode S-parameter representation of four-port.

It is useful to convert this model to a so-called mixed-mode model, shown in Figure 17. Indeed, tight coupling may exist between the input ports 1 and 2. Conversion from the conventional S-parameters to mixed-mode S-parameters can be done as follows. Denote with S_{STD} the matrix of the conventional S-parameters:

$$S_{STD} = \begin{pmatrix} S_{11} & S_{12} & S_{13} & S_{14} \\ S_{21} & S_{22} & S_{23} & S_{24} \\ S_{31} & S_{32} & S_{33} & S_{34} \\ S_{41} & S_{42} & S_{43} & S_{44} \end{pmatrix}, \qquad (18)$$

in which S_{ij}, 0<i,j<5 are the standard S-parameters. Denote with S_{MM} the matrix of the mixed-mode S-parameters:

$$S_{MM} = \begin{pmatrix} S_{DD11} & S_{DD12} & S_{DC11} & S_{DC12} \\ S_{DD21} & S_{DD22} & S_{DC21} & S_{DC22} \\ S_{CD11} & S_{CD12} & S_{CC11} & S_{CC12} \\ S_{CD21} & S_{CD22} & S_{CC21} & S_{CC22} \end{pmatrix} \tag{19}$$

In (19), subscript D refers to the differential port, subscript C to the common-mode port, 1 to the input port and 2 to the output port (see also Figure 17). It can be shown that the standard-mode S-parameters can be converted to the mixed-mode S-parameters using the following relationship:

$$S_{MM} = MS_{STD}M^{-1} \tag{20}$$

with M the matrix given by:

$$M = \frac{1}{\sqrt{2}} \begin{pmatrix} 1 & 0 & -1 & 0 \\ 0 & 1 & 0 & -1 \\ 1 & 0 & 1 & 0 \\ 0 & 1 & 0 & 1 \end{pmatrix}. \tag{21}$$

Of particular importance here are the differential input return loss S_{DD11} (reference impedance 100Ω, amount of reflected differential RF-power) and differential-to-common-mode conversion (reference impedance 25Ω, loss of differential RF-power due to conversion to common-mode RF power). Indeed, both these quantities describe the signal integrity of the differential input signal, which is the intended and useful signal here. Further, common-mode input return loss has been specified here as well.

Table 7 – Return loss specification of the input to the VCSEL driver.

Parameter	Min.	Typ.	Max.	Unit	Remarks
Differential return loss S_{DD11}			-10	dB	1GHz < f < 20GHz
			-8	dB	20GHz < f < 40GHz
Common-mode return loss S_{CC11}			-8	dB	1GHz < f < 40GHz
Differential-to-common-mode conversion S_{CD11}			-12	dB	1GHz < f < 40GHz

1.3.5. Specification of the optical output

The specification of the optical output is of course dependent on the used VCSEL. Therefore, the following specification serves as a guideline only. Its main purpose is to serve as a starting point to derive the specifications for the electrical output of the driver, based upon a reasonable range of VCSEL parameters such as threshold current, slope efficiency etc. Such derivation can be done using the methods explained in D5.1. Table 8 gives the target optical specification.

Table 8 – Target optical specifications.

Parameter	Min.	Typ.	Max.	Unit	Remarks
Average emitted optical power	-8		+1	dBm	
Optical modulation amplitude	-6		+3	dBm	
Extinction ratio	3			dB	

In a next step, we specify a range of VCSEL threshold currents and slope efficiencies, as well as threshold voltages and differential resistance. The VCSEL driver should be capable of generating bias and modulation currents such that the optical specifications from Table 8 are met. From Table 9, one can clearly note that a wide range of VCSEL parameters can be supported.

Table 9 – Supported VCSEL parameters.

Parameter	Min.	Typ.	Max.	Unit	Remarks
Threshold current	0.2		2.5	mA	
Slope efficiency	0.5		1	W/A	
Threshold voltage	1		2	V	
Differential resistance	50		100	Ω	

1.3.6. Specification of electrical output

Using the method as explained in D5.1, a range and accuracy of bias and modulation currents can be derived that allows to comply with the specifications in Table 8 using VCSELs with parameters set out in Table 9. A major difficulty is to predict the jitter in the optical output waveform. Indeed the current VCSEL samples still exhibit high amounts of jitter (distortion) at speeds above 30Gb/s. The exact amount of jitter is difficult to predict as the VCSEL samples are still in development. The approach therefore taken is to add additional functionality to the VCSEL driver to increase both the horizontal and vertical eye opening. This additional functionality consists of pulse width predistortion and selectable emphasis on the rising and falling edges of the driving waveform. The waveform is shown on Figure 18. Rising and falling edge pre-emphasis helps to compensate for the RC-limitations arising from the VCSEL parasitics. Further, falling edge pre-emphasis helps to accelerate the transition from a 1 to a 0 in the optical modulation response.

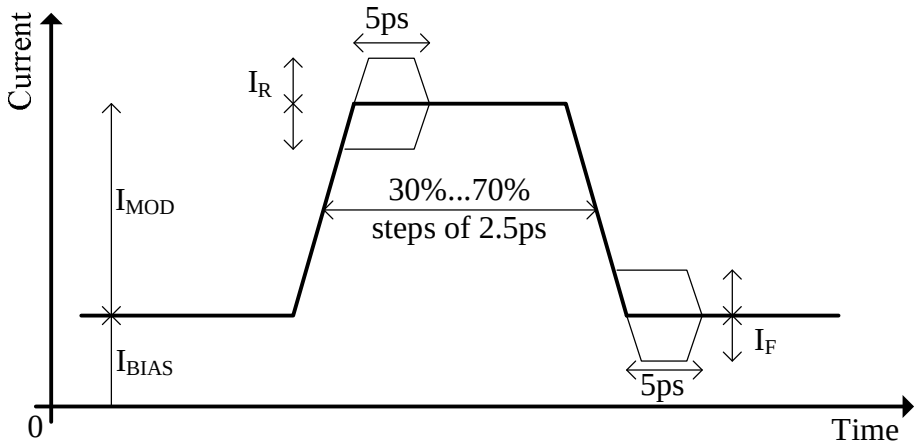


Figure 18 – Electrical output waveform with selectable emphasis.

The effect of rising edge pre-emphasis can be seen in Figure 19: note how the vertical eye opening is increased. The effect of different amounts and types of emphasis is further demonstrated in Table 10. No effect can be seen on the horizontal eye opening.

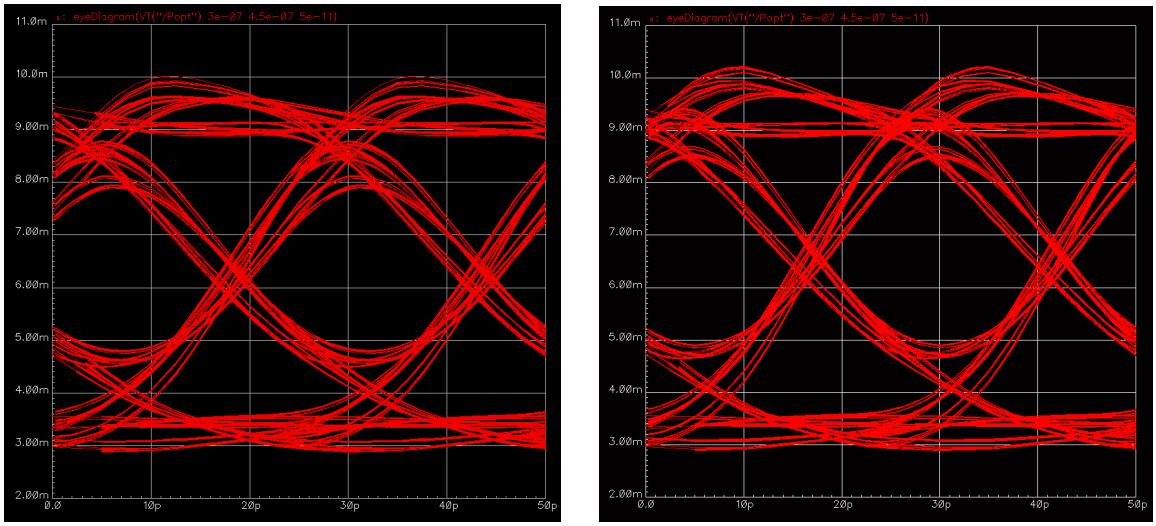


Figure 19 – No pre-emphasis (left) vs rising edge pre-emphasis (right) (I_{bias} = 7mA, I_{mod} = 10mA, I_R = 5mA, 40Gb/s).

Table 10 – Effect of emphasis.

Rising edge pre-emphasis (mA)	Falling edge pre-emphasis (mA)	Vertical eye opening (mW)	Horizontal eye opening (ps)
0	0	3.07	20.5
3	0	3.38	20.6
0	3	2.99	20.6
3	3	3.20	20.7
5	0	3.60	20.6

To improve the horizontal eye opening, the pulse width can be pre-distorted: see Figure 20. Note that increasing the pulse width reduces the vertical eye opening however. This can then be solved by adding falling edge emphasis, see Figure 21.

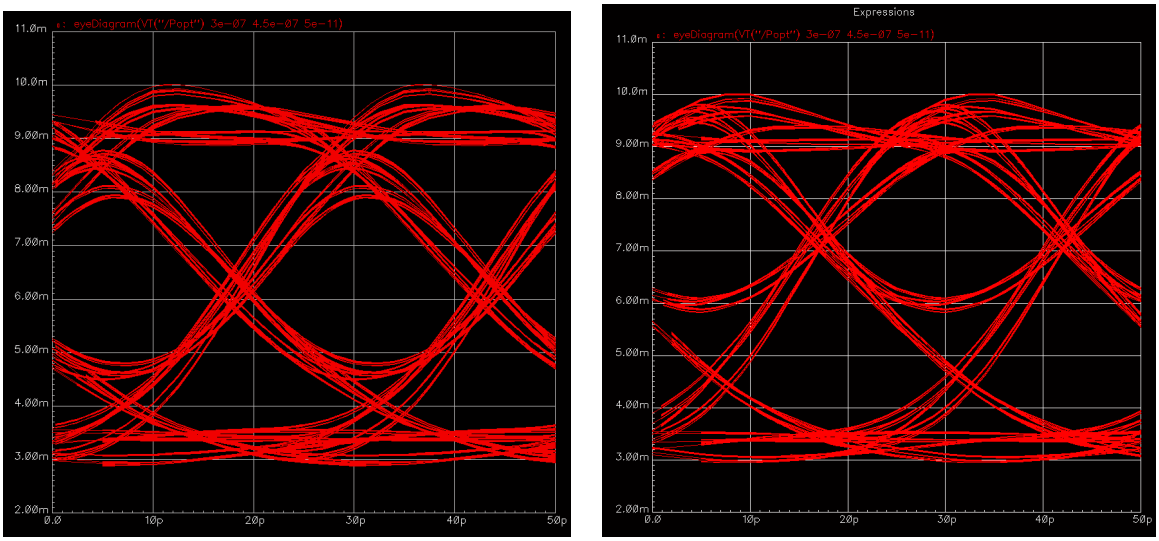


Figure 20 – No pre-distortion (left) vs pre-distortion added (right)
(I_{bias} = 7mA, I_{mod} = 10mA, applied pulse width = 65%, 40Gb/s).

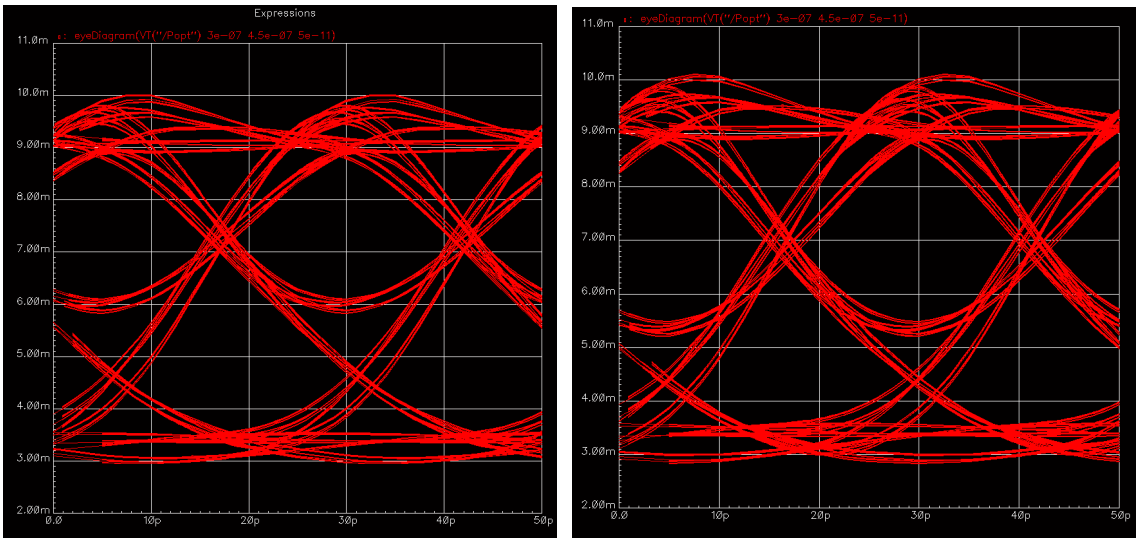


Figure 21 – Pure pre-distortion (left) vs pre-distortion combined with falling edge emphasis (right)
(I_{bias} = 7mA, I_{mod} = 10mA, I_F = 3mA, applied pulse width = 65%, 40Gb/s).

From the above simulations, it is obvious that the optimum emphasis and pulse width pre-distortion settings are highly dependent upon the actual VCSEL parameters. As these are not yet known and may vary widely from one VCSEL sample to another, it was decided to implement a VCSEL driver with adjustable emphasis and pre-distortion settings. Further, all the settings will be digitally programmable, which allows to control the emphasis and predistortion settings using externally added feedback loops if so required. Table 11 gives the details of all the parameters of the electrical output.

Table 11 – Specifications on the electrical output waveform.

Parameter	Min.	Typ.	Max.	Unit	Remarks
BIAS CURRENT (I_{BIAS})					
Full-scale current I_{BIASFS}		5.1		mA	+/- 5%
Resolution		20		µA	
Integral non-linearity		+/- 1		LSB	
Differential non-linearity		+/- 1		LSB	
MODULATION CURRENT (I_{MOD})					
Full-scale current I_{MODFS}		25.5		mA	+/- 5%
Resolution		100		µA	
Integral non-linearity		+/- 1		LSB	
Differential non-linearity		+/- 1		LSB	
Width rising edge emphasis pulse		5		ps	
Width falling edge emphasis pulse		5		ps	
Rise time (20% to 80%)		5		ps	Emphasis off
Fall time (20% to 80%)		5		ps	Emphasis off
Data eye crossing point range	30	50	70	%	@ 40Gb/s: 50%=25ps
Data eye crossing point resolution		2.5		ps	
Random jitter		5		ps p-p	
RISING EDGE PRE-EMPHASIS I_R					
Full-scale current I_{RFS}		3.75		mA	+/- 5%
Resolution		250		µA	
Integral non-linearity		+/- 1		LSB	
Differential non-linearity		+/- 1		LSB	
RISING EDGE DE-EMPHASIS I_R					
Full-scale current I_{RFS}		3.75		mA	+/- 5%
Resolution		250		µA	
Integral non-linearity		+/- 1		LSB	
Differential non-linearity		+/- 1		LSB	
FALLING EDGE PRE-EMPHASIS I_F					
Full-scale current I_{FFS}		3.75		mA	+/- 5%
Resolution		250		µA	
Integral non-linearity		+/- 1		LSB	
Differential non-linearity		+/- 1		LSB	
FALLING EDGE DE-EMPHASIS I_F					
Full-scale current I_{FFS}		3.75		mA	+/- 5%
Resolution		250		µA	
Integral non-linearity		+/- 1		LSB	
Differential non-linearity		+/- 1		LSB	

1.3.7. Specification of input equalizer

As a result of dielectric losses and skin-effect in conductors, RF losses at frequencies above 10GHz can be substantial. RF losses are frequency dependent and hence may introduce a significant amount of intersymbol interference and jitter. Therefore the VCSEL driver will include a settable equalizer to compensate for such losses. For example, Figure 22 shows the insertion loss (S_{21}) of a 5cm trace on a PCB (Rogers R4003 dielectric): almost 3dB loss at 40GHz can be observed. Further losses can be incurred by coaxial cables used for testing purposes, connectors etc. Therefore, a programmable equalizer will be foreseen on-chip which will provide up to 10dB peaking at 20GHz, programmable in 1dB steps.

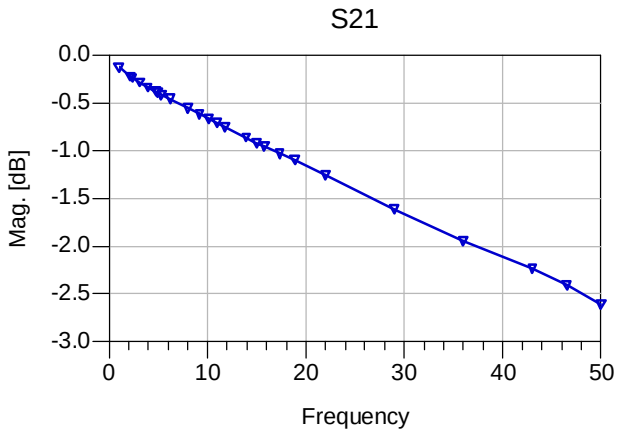


Figure 22 – Insertion loss of a 5cm 50Ω microstrip on Rogers RO4003 dielectric.

1.4. Driver circuitry

1.4.1. Detailed circuit topology

The detailed architecture of the driver is shown in Figure 23. It mainly consists of three differential pairs, that steer the modulation current either to the VCSEL (for a logical 1) or to a dummy resistor (for a logical 0). The uppermost differential pair switches the modulation current, while the two lower differential pairs switch the adjustable rising and falling edge emphasis currents. All currents are generated using D/A converters (DACs) with current output. Pre- or de-emphasis is generated by subtracting the adjustable emphasis current (ranging from 0 to $2I_{FullScale}$) from the full-scale current $I_{FullScale}$. Appropriate scaling in the current mirrors will be used to minimize power consumption. The uppermost differential pair is switched by the pre-distorted input signal.

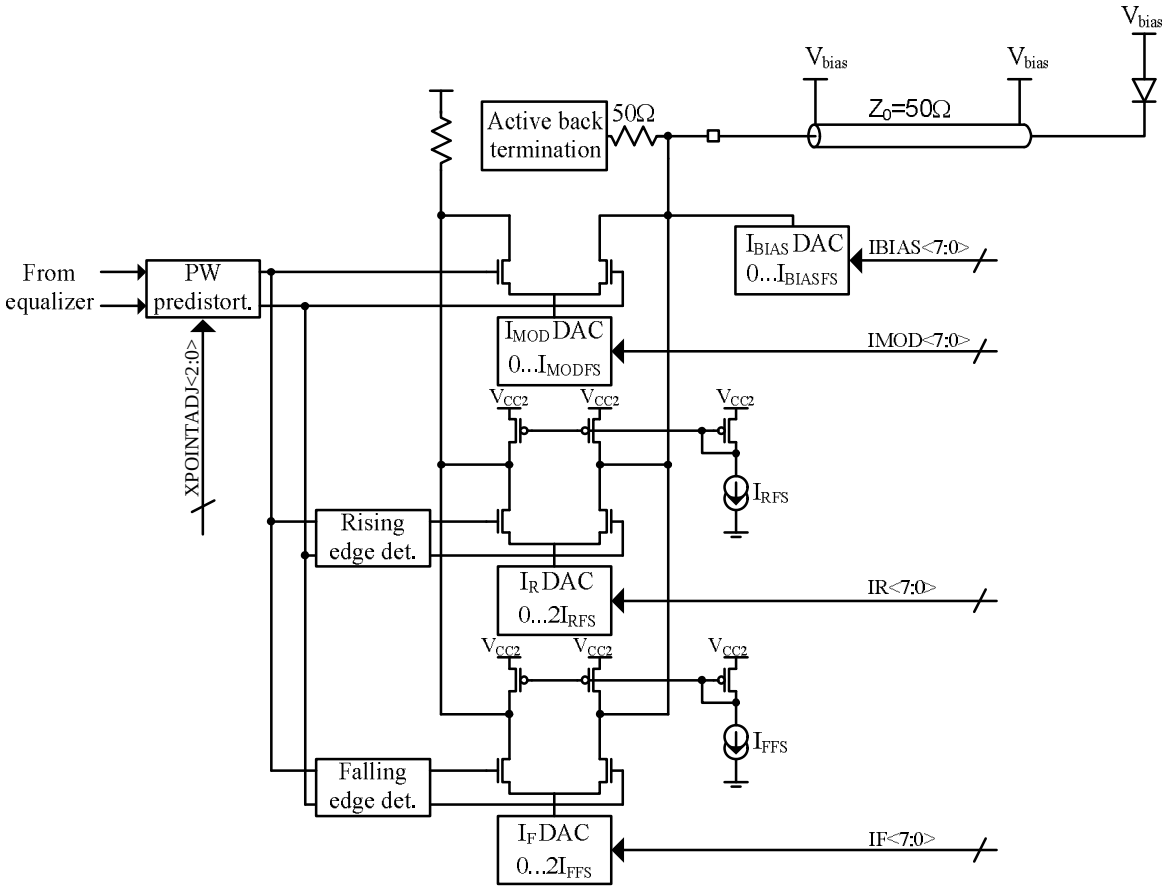


Figure 23 – Architecture of the VCSEL driver.

The emphasis differential pairs are controlled by respectively a rising edge detector and a falling edge detector, whose operation is shown in Figure 24. Note that the required logic gates need to have a very high bandwidth (~30GHz) for 40Gb/s. Standard CMOS logical gates are not fast enough. Moreover, note that usage of CMOS logical gates would require to convert the CML-like input to a full-swing logical CMOS signal, and then back again to a CML-like signal swings to steer the emphasis differential pairs. Therefore, it was decided to develop MOS current-mode logic gates (MCML).

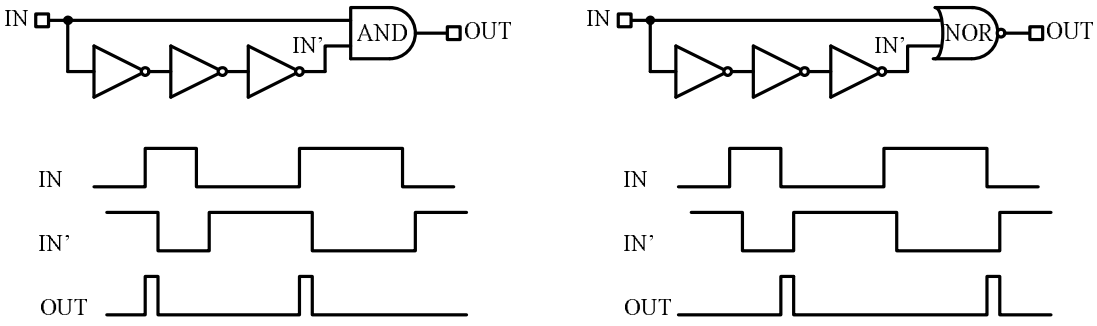


Figure 24 – Schematic and operation of the rising edge detector (left) and falling edge detector (right).

Two possibilities are currently under consideration: gates using passive or active inductors. Gates based upon active inductors offer the advantage of minimum area requirements at the expense higher power consumption for the same gate delay and rise time. Passive inductors may reduce the rise time further, at the expense of increased die area.

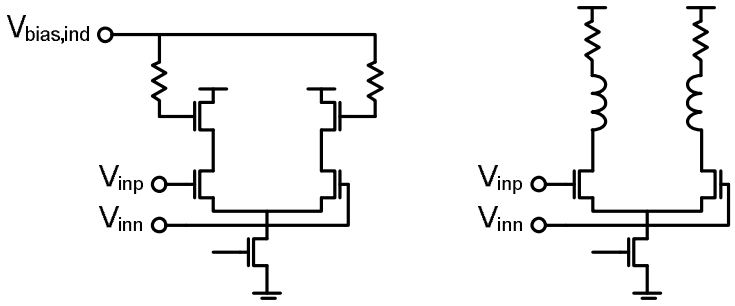


Figure 25 – MCML inverter gates using active inductors (left) or passive inductors (right).

1.4.2. Common-anode configuration

Due to the low available supply voltage for the driver (1.2V - 1.8V) a common-anode configuration has been selected. For the current type of VCSELs (n-type substrate, see Figure 26) this has one disadvantage: the driver needs to handle the additional capacitance of the mounting metal to ground. Clearly, a detailed model is needed to estimate the value of this capacitance, which is one of the reasons to use electromagnetic simulators to generate an equivalent model of the VCSEL parasitics.

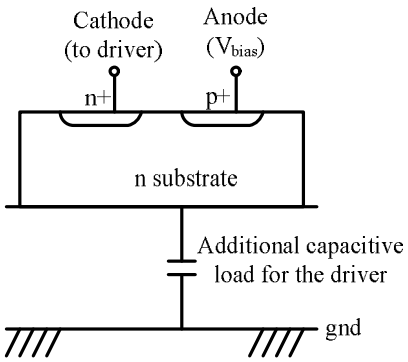


Figure 26 – Common-anode driven VCSEL: additional capacitance due to mounting plate.

This capacitance has been estimated to be roughly 150fF. The magnitude of this capacitance is sufficient to limit the bandwidth at 40Gb/s, hence it is expected that inductive peaking will be required at the driver output.

1.4.3. Active back termination

An important consideration is the output return loss of the driver. Indeed given the high bandwidth, the interconnection between the driver and the VCSEL needs to be designed with a controlled characteristic impedance. As the impedance of the VCSEL itself is not well defined, signal integrity then requires that the output of the driver has good output return loss. This can be easily achieved using a parallel termination resistor matched to the characteristic impedance of the transmission line interconnection to the VCSEL. However such a termination resistor not only puts additional requirements on the VCSEL driver (the driver must now supply current to both this termination resistor and the VCSEL) it also increases power consumption. An elegant solution to avoid this additional power consumption consists of so-called active back termination, see Figure 27 [5]. Instead of connecting the termination resistor to a fixed bias voltage, it is connected to a voltage source that generates the intended voltage $v_0(t)$ at the output of the VCSEL (assuming no reflections). Note that in the ideal case (no reflections) no power is wasted in this termination resistor. If reflections do occur (e.g. if the VCSEL impedance is different from the characteristic impedance of the interconnection) these will be absorbed by the voltage source. Hence, the voltage source can be designed as a unity gain buffer that only needs to supply sufficient current to be able to absorb any back reflections from the VCSEL load.

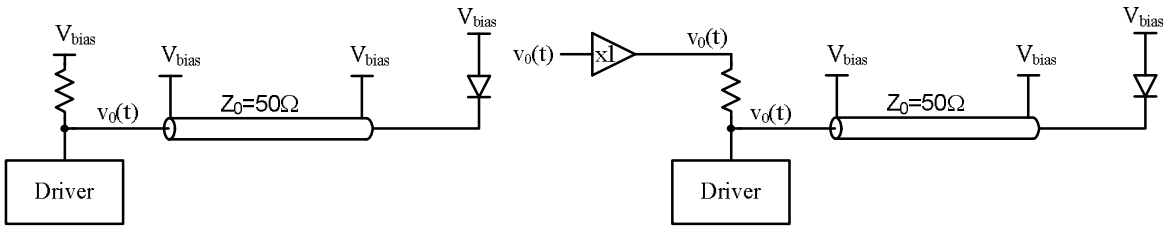


Figure 27 – Passive termination (left) and active termination (right) – $v_0(t)$ is the driver output voltage in case the VCSEL impedance equals the characteristic impedance of the transmission line.

1.5. Preliminary simulation results

A first design of the output driver switching transistors has been done. Figure 28 shows how good (optical) eye openings can be obtained, as well as output driver currents with extremely fast rising and falling edges. It is also shown that pre-emphasis can be added, and further that this helps to increase the vertical eye opening.

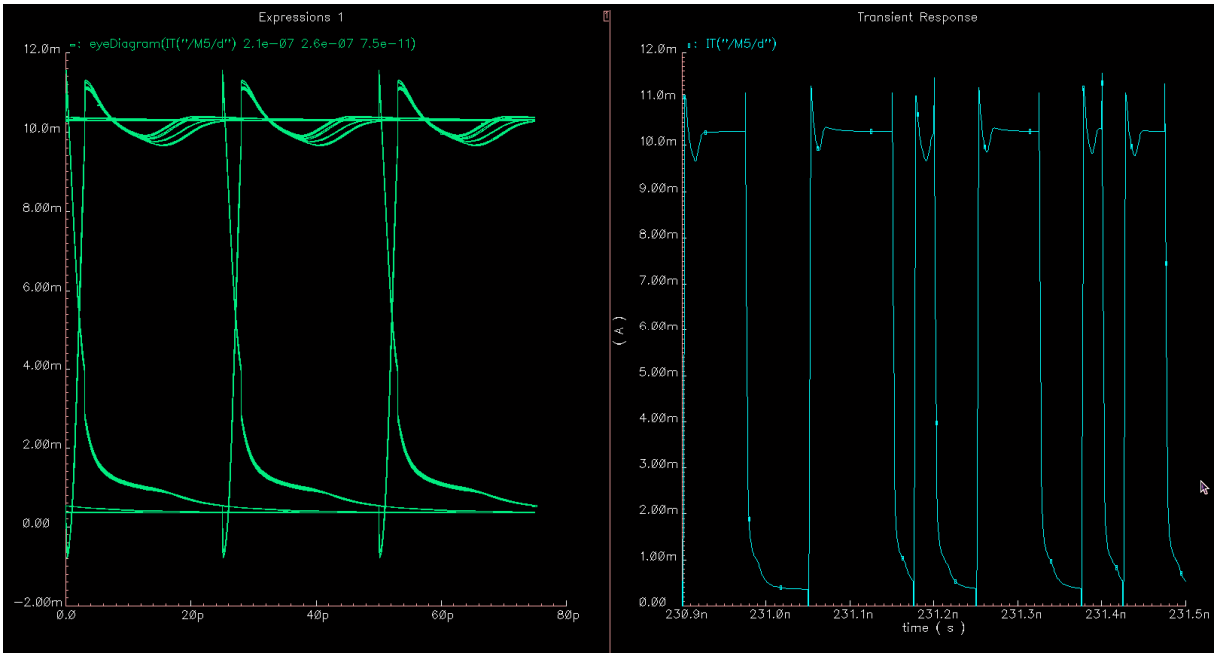


Figure 28a – Modulation current waveforms.

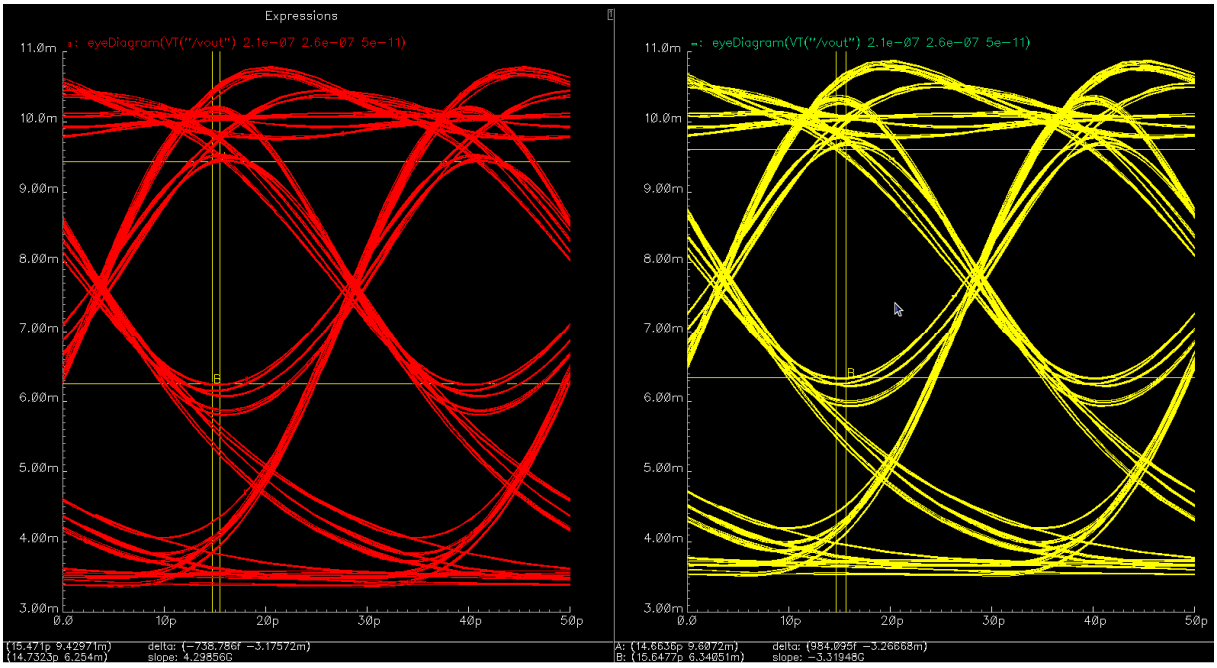


Figure 28b – Current waveforms.

1.6. Conclusion

The main specifications for a 40Gb/s VCSEL driver have been presented. The feasibility to design it in a 65nm CMOS technology has been shown. Improvement of eye quality will be done by adding advanced features to the VCSEL driver such as programmable pre- or de-emphasis.

The next steps in the design work will involve putting together a suitable model of the used packaging method, and co-designing the driver with this model.

2. Modulation formats for the VISIT project

The continuing rise in traffic in local-area networks is motivating the development of new standards for datacommunication links. For example, IEEE 802.3 is currently finalizing the standardization of the initial forms of 40 Gigabit Ethernet and 100 Gigabit Ethernet. In contrast to previous standards, such as 10 Gigabit Ethernet, operation at 40 Gb/s and beyond necessitates multiplexing of several lower-rate channels, e.g. at 10 Gb/s, to achieve high aggregate line rates at a commercially acceptable cost. Indeed, the standards under development are considering the application of multiple optical channels, through the application of wavelength-division multiplexing. However, it would be preferable to employ multiple electrical channels on a *single optical wavelength*, thereby avoiding the cost of multiple lasers, photodetectors and the associated optical multiplexing components.

This section discusses the types of modulation formats that are relevant to this goal. Simulation results are presented at a wavelength of 850nm, relevant to the vertical-cavity surface-emitting lasers (VCSELs) developed in VISIT. Transmission over OM3 multimode fibre (MMF) is considered, since it is the most relevant medium for current datacommunication links. Results are presented for an aggregate data rate of 20 Gb/s, with bandwidth assumptions for the optical source chosen to be compatible with the VCSELs under consideration within VISIT.

The trade-offs between the different modulation formats are considered in terms of link length, receiver sensitivity and complexity of implementation. For example, some advanced modulation formats offer increased spectral efficiency and therefore the ability to use lower bandwidth devices, but with greater requirements in terms of signal-to-noise ratio, the linearity of the optical source and the complexity of the associated electronics.

2.1. Non-return-to-zero modulation

Non-return-to-zero (NRZ) modulation is the simplest modulation format under consideration, being simply pulse-amplitude modulation (PAM) with two levels. The main advantages relative to the other modulation formats under consideration here are: (i) low-complexity transmitter and receiver electronics; (ii) good receiver sensitivity. The main disadvantage is poor spectral efficiency and therefore greater dependency on the speed of the optical source.

Figure 29(a) shows a typical back-to-back NRZ eye diagram at 20 Gb/s, assuming a 23.5 ps rise time (20% to 80%) of the optical source (with a Gaussian pulse shape) and a –3 dBe bandwidth of 15 GHz for the receiver electrical filter (with a 4^{th}-order Bessel-Thomson response). A $2^7 – 1$ pseudo random binary sequence (PRBS) is used to model the short-run-length line codes commonly used in datacommunication links. Figure 29(b) shows the result of a statistical consideration of transmission over OM3 MMF, in which a worst-case model of this transmission medium is considered.

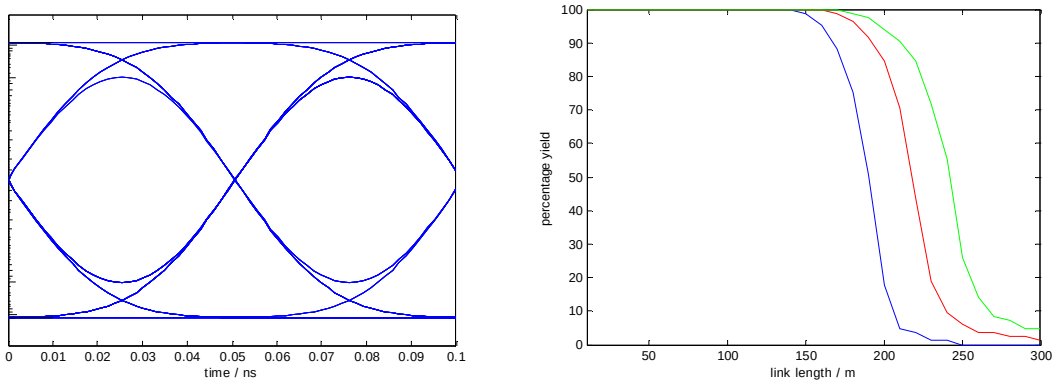


Figure 29(a) Back-to-back NRZ eye diagram at 20 Gb/s; (b) percentage yield of worst-case OM3 links at 20 Gb/s, where the blue, red and yellow lines correspond to 3 dBo, 4 dBo and 5 dBo maximum dispersion penalty criteria, respectively.

The variations in refractive-index profile and launch conditions are taken into account such that this model represents the worst 5% of installed links; therefore a percentage yield of 80% corresponds to 99% of the installed base. The results therefore indicate potential link lengths of 175m (at 3dBo maximum dispersion penalty), 205m (at 4dBo maximum dispersion penalty) and 225m (at 5dBo maximum dispersion penalty).

Considering receiver sensitivity, it is found that a back-to-back sensitivity of –16.7dBm is possible. This assumes a thermal-noise-dominated receiver with identical noise power spectral density to that which gives rise to a sensitivity of –18.0dBm for a 10.3125Gb/s reference receiver with a 47.1ps rise time (20% to 80%) of the optical source (with a Gaussian pulse shape) and a –3 dBe bandwidth of 7.5GHz for the receiver electrical filter (with a 4^{th}-order Bessel-Thomson response). This reference noise power spectral density is used throughout to allow comparison of the performance of the different modulation formats. The sensitivity is calculated at a bit-error ratio of 10^{-12} and assuming a p-i-n photodetector with a responsivity of $0.9AW^{-1}$.

The potential advantage of electronic equalisation in the receiver is also considered. It is found that a 7-tap feed-forward equaliser (FFE) extends the link length to 250 m (at 4 dBo maximum dispersion penalty). The FFE tap spacing is assumed to be one symbol period, i.e. 50 ps.

2.2. Pulse-amplitude modulation (4 levels)

As indicated in section 2.1, NRZ modulation is a special case of PAM, where the number of levels is two and therefore the symbol rate and the bit rate are identical. In this section, we consider PAM with four levels (PAM4), such that each symbol represents two bits and the symbol rate is therefore one half of the bit rate. This reduction in symbol rate, e.g. 10 Gbaud for a 20 Gb/s link, implies an advantage in spectral efficiency relative to NRZ modulation. Therefore, optical sources with reduced bandwidth compared to a NRZ link may be

employed. The main disadvantages are: (i) greater complexity of the transmitter and receiver electronics; (ii) degraded receiver sensitivity since, for a given received optical power, the effective optical modulation amplitude for each eye within the PAM4 waveform is approximately one third of that available to the NRZ receiver.

Figure 30(a) shows a typical back-to-back PAM4 eye diagram at 20 Gb/s, assuming a 35 ps rise time (20% to 80%) of the optical source (with a Gaussian pulse shape) and a –3 dBe bandwidth of 7.5 GHz for the receiver electrical filter (with a 4^{th}-order Bessel-Thomson response). As before, a $2^7 - 1$ PRBS is used to model the short-run-length line codes commonly used in datacommunication links. Figure 30(b) shows the result of a statistical consideration of transmission over OM3 MMF, in which, as before, a worst-case model of this transmission medium is considered.

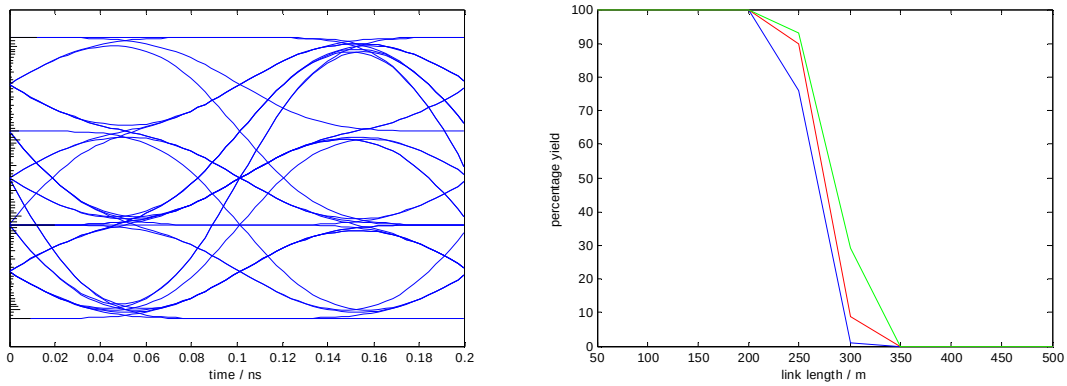


Figure 30(a) Back-to-back PAM4 eye diagram at 20 Gb/s; (b) percentage yield of worst-case OM3 links at 20 Gb/s, where the blue, red and yellow lines correspond to 3 dBo, 4 dBo and 5 dBo maximum dispersion penalty criteria, respectively.

The results indicate potential link lengths of 245 m (at 3 dBo maximum dispersion penalty), 255 m (at 4 dBo maximum dispersion penalty) and 260 m (at 5 dBo maximum dispersion penalty).

Considering receiver sensitivity, it is found that a back-to-back sensitivity of –12.1 dBm is possible, assuming the reference noise power spectral density described in section 2.1.

The potential advantage of electronic equalisation in the receiver is considered. It is found that a 7-tap feed-forward equaliser (FFE) extends the link length to 500 m (at 4 dBo maximum dispersion penalty). The FFE tap spacing is assumed to be one symbol period, i.e. 100 ps.

In conclusion, even though lower-speed optical sources have been considered, the potential link lengths with PAM4 are significantly higher than for NRZ modulation. However, there is a 4.6 dBo degradation in receiver sensitivity relative to NRZ modulation. Also, the use of multilevel modulation formats imposes greater linearity requirements on the optical source.

2.3. Duobinary modulation

Duobinary modulation is based on a form of partial-response encoding in which three-level symbols are employed in such a way that improved spectral efficiency is achieved, although

the symbol rate and the bit rate remain identical as in NRZ modulation. The improved spectral efficiency results in greater tolerance to intersymbol interference and therefore reduced dispersion penalty. However, there is a degradation in receiver sensitivity relative to NRZ modulation, for the same reason as for PAM4.

Figure 31(a) shows a typical back-to-back duobinary eye diagram at 20 Gb/s, assuming a 23.5 ps rise time (20% to 80%) of the optical source (with a Gaussian pulse shape) and a –3 dBe bandwidth of 7.5 GHz for the receiver electrical filter (with a 4th-order Bessel-Thomson response). As before, a 2^7 – 1 PRBS is used to model the short-run-length line codes commonly used in datacommunication links. Figure 31(b) shows the result of a statistical consideration of transmission over OM3 MMF, in which, as before, a worst-case model of this transmission medium is considered.

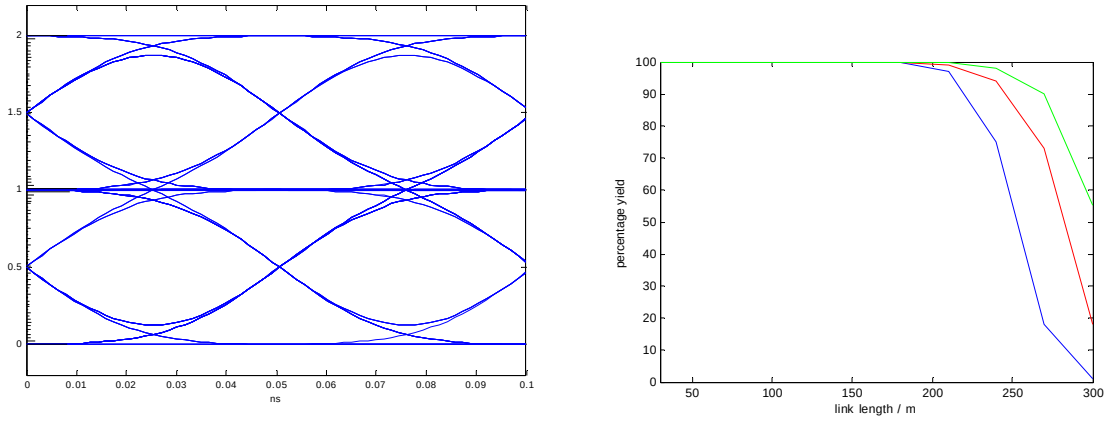


Figure 31(a) Back-to-back duobinary eye diagram at 20 Gb/s; (b) percentage yield of worst-case OM3 links at 20 Gb/s, where the blue, red and yellow lines correspond to 3 dBo, 4 dBo and 5 dBo maximum dispersion penalty criteria, respectively.

The results indicate potential link lengths of 235 m (at 3 dBo maximum dispersion penalty), 260 m (at 4 dBo maximum dispersion penalty) and 280 m (at 5 dBo maximum dispersion penalty).

Considering receiver sensitivity, it is found that a back-to-back sensitivity of –13.7 dBm is possible, assuming the reference noise power spectral density described in section 2.1.

In conclusion, a significant advantage in link length is possible with duobinary modulation relative to NRZ modulation. However, there is a 3.0 dBo degradation in receiver sensitivity relative to NRZ modulation.

2.4. Quadrature phase-shift keying

Instead of a single high-data-rate channel, the use of multiple channels, each corresponding to a particular microwave carrier frequency, may be considered. In this section, a 20 Gb/s quadrature-phase-shift-keyed (QPSK) scheme is considered, in which four 5 Gb/s channels are electrically combined in the transmitter. Each 5 Gb/s channel is formed from two 2.5 Gb/s NRZ data streams that phase modulate a local oscillator in quadrature. The advantages of such an approach include: (i) the ability to adjust the spectrum depending on the frequency

response of the transmission medium; (ii) good receiver sensitivity, due to the coherent nature of the detection in the microwave domain.

Figure 32(a) shows a typical four-channel QPSK electrical spectrum at 20 Gb/s. Figure 32(b) shows the result of a statistical consideration of transmission over OM3 MMF, in which, as before, a worst-case model of this transmission medium is considered. We again assume a 23.5 ps rise time (20% to 80%) of the optical source (with a Gaussian pulse shape) although with a –3 dB bandwidth of 18 GHz for the receiver electrical filter (with a 4^{th}-order Bessel-Thomson response). As before, a $2^7 – 1$ PRBS is used to model the short-run-length line codes commonly used in datacommunication links.

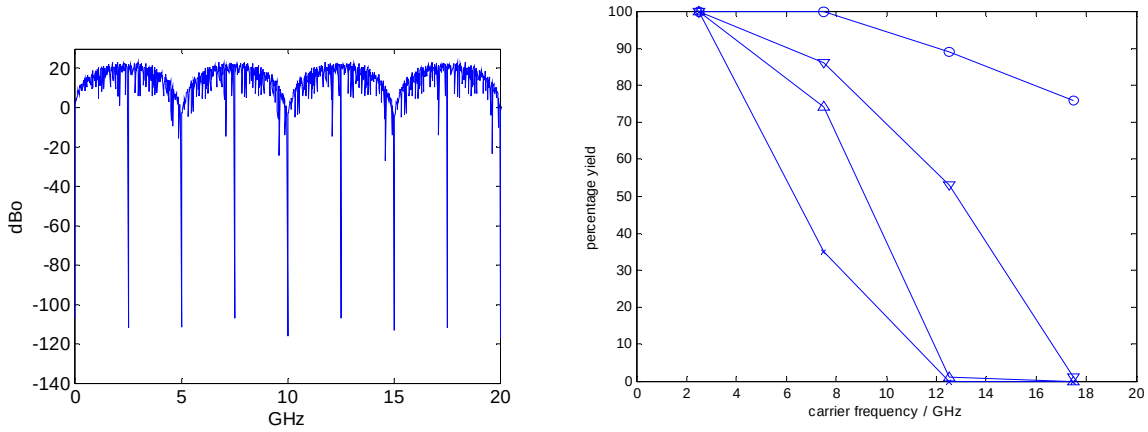


Figure 32(a) Four-channel QPSK electrical spectrum at 20 Gb/s; (b) percentage yield of worst-case OM3 links at 20 Gb/s, for link lengths of 300 m (circles), 500 m (downward-pointing triangles), 700 m (upward-pointing triangles) and 900 m (crosses).

The results in Figure 32(b) are based upon a maximum dispersion penalty criterion of 2 dBo and a maximum RF attenuation of 12 dBo. A link length of 300 m is observed to be feasible.

Considering receiver sensitivity, it is found that a back-to-back sensitivity of –17.6 dBm is possible, assuming the reference power spectral density described in section 2.1.

In conclusion, a significant advantage in link length is possible with this multichannel QPSK approach relative to NRZ modulation. In addition, there is a 0.9 dBo enhancement in receiver sensitivity relative to NRZ modulation. However, the additional complexity of the transmitter and receiver electronics is significant. RF attenuation at each carrier frequency due to the MMF frequency response must also be considered.

2.5. Quadrature amplitude modulation

Finally, we consider a similar approach to that of section 2.4, except that 20 channels are employed, each of which is a quadrature-amplitude-modulated (QAM) channel with a data rate of 1 Gb/s. QAM16 is chosen, such that each channel is formed from two 500 Mb/s PAM4 data streams that phase modulate a local oscillator in quadrature.

Fig. 33(a) shows a typical 20-channel QAM16 electrical spectrum at 20 Gb/s. Fig. 33(b) shows the result of a statistical consideration of transmission over OM3 MMF, in which, as before, a worst-case model of this transmission medium is considered. We again assume a 23.5 ps rise time (20% to 80%) of the optical source (with a Gaussian pulse shape) with a –3 dB bandwidth of 18 GHz for the receiver electrical filter (with a 4^{th}-order Bessel-Thomson response). As before, a $2^7 - 1$ PRBS is used to model the short-run-length line codes commonly used in datacommunication links.

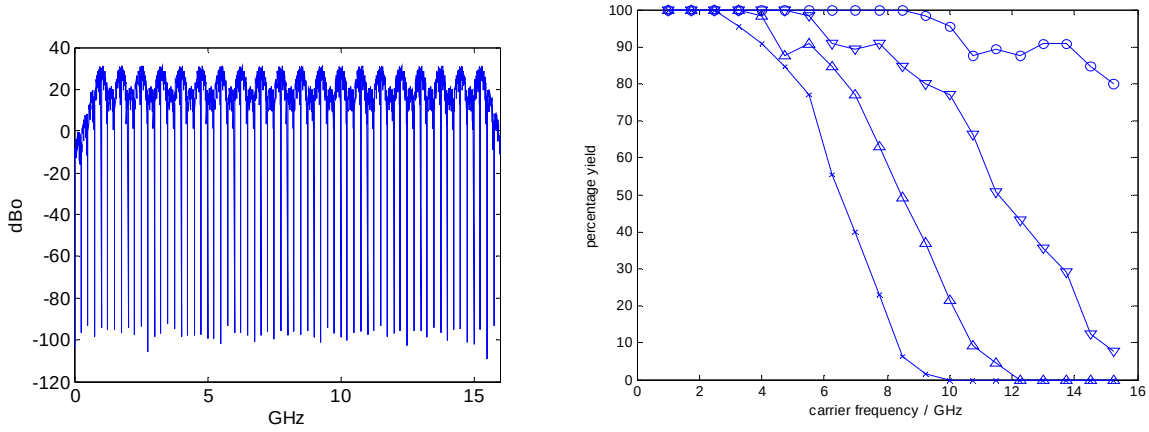


Figure 33(a) 20-channel QAM16 electrical spectrum at 20 Gb/s; (b) percentage yield of worst-case OM3 links at 20 Gb/s, for link lengths of 300 m (circles), 500 m (downward-pointing triangles), 700 m (upward-pointing triangles) and 900 m (crosses).

The results in Figure 33(b) are based upon a maximum dispersion penalty criterion of 2 dBo and a maximum RF attenuation of 12 dBo. A link length of 300 m is observed to be feasible.
Considering receiver sensitivity, it is found that a back-to-back sensitivity of –16.5 dBm is possible, assuming the reference power spectral density described in section 2.1.
In conclusion, a significant advantage in link length is possible with this multichannel QAM16 approach relative to NRZ modulation. However, there is a 0.2 dBo degradation in receiver sensitivity relative to NRZ modulation. As for QPSK, the additional complexity of the transmitter and receiver electronics is significant. RF attenuation at each carrier frequency due to the MMF frequency response must also be considered.

2.6. Receiver Characteristics

In order to achieve a bit rate of 40 Gb/s with appreciable link margin the achievable receiver sensitivity is an important factor. GaAs is typically the material of choice for p-i-n photodiodes at 850 nm because of its ease of design, and its excellent operating characteristics such as low dark current, high bandwidth, and almost 100% quantum efficiency [6]. The back-to-back sensitivity (at a bit-error ratio of 10^{-12}) of a 40Gb/s receiver assuming an ideal GaAs device with a 100% quantum efficiency (corresponding to a responsivity of 0.7 A/W at

840 nm) is -14.6dBm. This assumes a thermal-noise-dominated receiver with a 15pA/Hz$^{1/2}$ noise current spectral density for a 40 Gb/s bit rate with a 12 ps rise time (20% to 80%) of the optical source (with a Gaussian pulse shape) and a –3 dBe bandwidth of 30 GHz for the receiver electrical filter (with a 4th-order Bessel-Thomson response). Currently there are PIN detectors available which have responsivity values ~0.4 A/W, thus reducing the receiver sensitivity from the ideal of -14.6 dBm to -12.2 dBm. Given the low responsivity of the photodiode (limited predominantly by the wavelength of operation) as well as the limited available transimpedance gain (due to the high operating bitrate) an additional electrical amplifier is required to provide sufficient gain such that the resulting signal can be provided to a subsequent clock-and-data recovery chip. The noise figure of this electrical amplifier can seriously degrade the overall receiver sensitivity of the link. A noise figure of 3.5 dB, degrades the overall sensitivity of the ideal receiver to -12.9 dBm. One method to achieve an improvement in receiver sensitivity is to utilise avalanche multiplication, however this technology is not yet available at the high bitrate of 40 Gb/s at 850 nm. In the mean-time as stated previously extended reach links can be implemented by using multilevel formats, OM4 fibre and/or equalisation techniques.

2.7. Conclusion

Several modulation formats with potential relevance to VISIT have been reviewed. It is found that there is a significant trade-off between the complexity of implementation and the resulting performance. Relative to NRZ modulation, PAM4 offers an extended link length, even when employing an optical source of reduced bandwidth. However, the degradation in receiver sensitivity is significant, especially in links with a highly-restricted power budget, which is typical for datacommunication systems operating at a wavelength of 850 nm. Duobinary modulation can be viewed as offering intermediate performance between NRZ modulation and PAM4. The use of multichannel QPSK and QAM16 schemes offers significantly increased link length compared to NRZ modulation and without degradation in receiver sensitivity. However, RF attenuation due to the MMF frequency response can render construction of a realistic power budget difficult. Furthermore, the complexity and potential difficulty of integration of the transmitter and receiver electronics are significant. As a final point, receiver electronic equalisation can provide a low-cost route to link length extension.
These observations are expected to continue to be relevant at higher data rates and suggest that, of the modulation formats considered here, NRZ modulation and PAM4 are of the greatest relevance to VISIT.

3. Analogue performance

3.1. Introduction

The analogue performance of a VCSEL must be considered if it is to be employed in applications such as Radio over Fibre (RoF) links. The performance of such a link can be measured using an Error Vector Magnitude (EVM) test. Another characteristic the device itself must show is good linearity. This can be measured by determining the spurious free dynamic range (SFDR).

The SFDR is a measure of the device's fidelity. Under ideal conditions, the frequency domain of an analogue signal has all its power concentrated at the fundamental frequency. But due to the nonlinearity within the device, frequency content is also generated at harmonics of this frequency, known as spurs. The strength of the signal at the harmonics is dependant on the non linearity of the device. This is illustrated further in Figure 34.

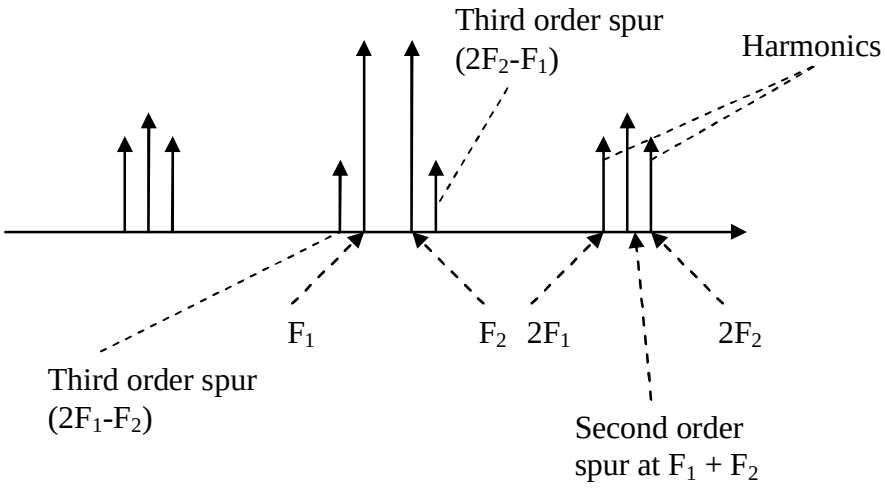


Figure 34 - Origin of the spurs.

When two frequencies are injected into a system, non linear interaction between them creates new signals at the sum and difference frequencies of the two fundamental tones. These are known as second order effects. In addition to these, non linear interaction between the fundamental tones and the harmonics produce third order spurs which occur at frequencies very near the fundamental tones and are usually inside the pass band of the system. In a RoF link, these distortions quickly give rise to increased bit error rates [7].

The range between the fundamental frequency and the largest spur is known as the SFDR. Analogue optical links used for distributing wireless signals such as 3G and IEEE 802.11 require devices with good linear performance. These RoF applications typically require SFDR values of 80dB.Hz$^{2/3}$ [8].

EVM is primarily a measure of the signal quality, providing a simple, quantitative figure-of-merit for a digitally modulated signal. It is defined as the vector difference at a given time between the measured signal and the ideal reference signal and can be expressed as a percentage. The IEEE 802.11 standard commonly used in EVM tests specifies a tolerance limit of 5.6% [9].

A list of applications which could be distributed through RoF and their associated frequencies is shown in Table 12.

Table 12 – Applications which could be distributed through RoF.

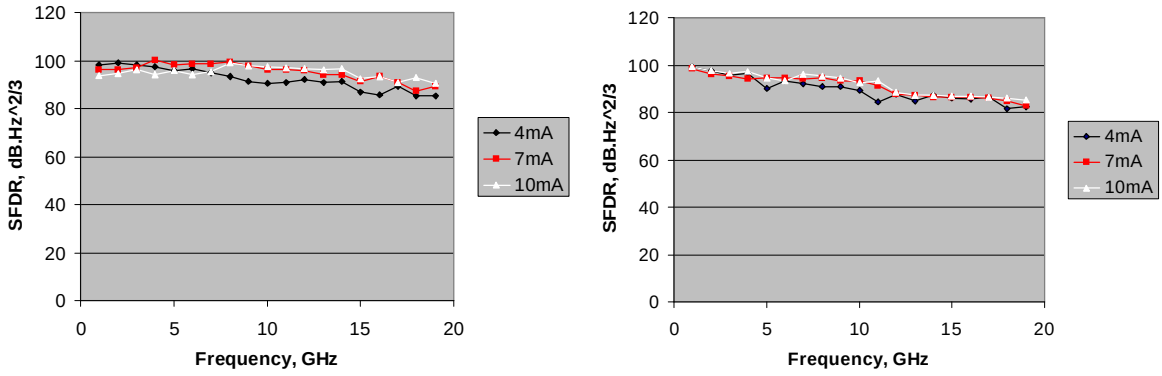
Application	Carrier Frequency
3G	1.9 GHz, 2.1 GHz
IEEE 802.11g (Wi-Fi)	2.4 GHz, 5 GHz
WiMax	2.3-2.5 GHz, 3.4-3.5 GHz

Future ultra-wideband (UWB) applications such as wireless USB and wireless video distribution would require carrier frequencies between 3.1 GHz to 10.6 GHz. Lasers capable of supporting those carrier frequencies would need to be used in such RoF links.

These tests were carried out on both the Chalmers and VI Systems (VIS) VCSELs. The Chalmers device selected for the test had an oxide aperture of 13µm. This device was selected due to it having the highest modulation bandwidth of the Chalmers' devices. For the same reason, the VIS device selected was the one with a mesa diameter of 28µm. The bandwidth of the two devices at 25°C was around 15GHz and 20GHz respectively.

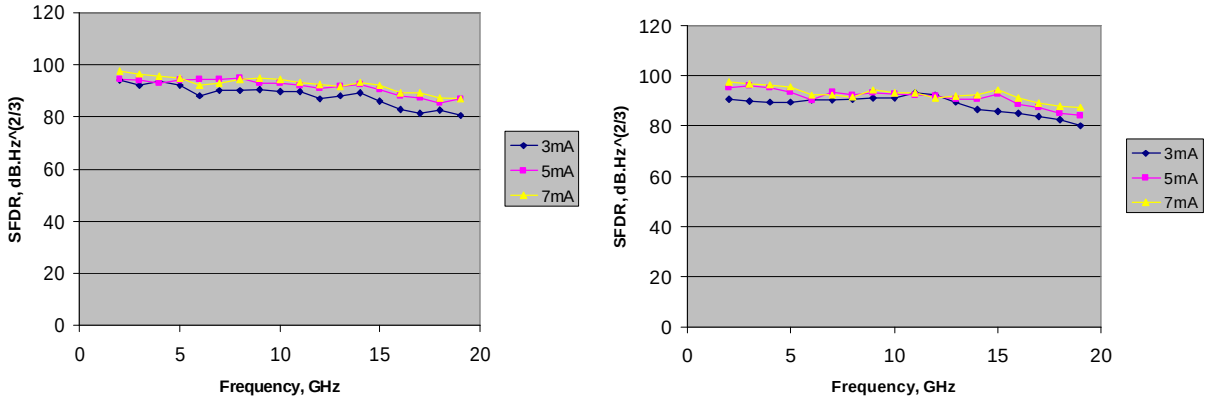
3.2. SFDR measurements

A standard two tone intermodulation test was carried out to measure the SFDR of the two devices. Two RF tones, separated in frequency by 1MHz, were combined using an RF splitter and then used to directly modulate the devices. This test was performed on the VIS device with bias currents of 4mA, 7mA and 10mA at 25°C and 70°C. On the Chalmers device, the same test was carried out at 3mA, 5mA and 7mA at 25°C and 70°C. The SFDR of the VIS device is shown in Figure 35a.



(a) (b)

Figure 35 - SFDR of 28µm mesa diameter VIS VCSEL at 25°C (a) and 70°C (b)



(a) (b)

Figure 36 - SFDR of 13µm oxide aperture Chalmers VCSEL at 25°C (a) and 70°C (b)

This device had a peak SFDR value greater than 100dB.Hz$^{2/3}$ with values consistently above 85dB.Hz$^{2/3}$ at frequencies up to 20GHz. This is a typical SFDR value required for a device to support next generation RoF applications. The Chalmers device performed similarly in this test, achieving SFDR values above 85dB.Hz$^{2/3}$ at frequencies up to 20GHz. Both devices demonstrated low temperature dependence in these tests. The SFDR of the Chalmers device is shown in Figure 36b.

3.3. EVM measurements

The EVM of an optical link was measured using IEEE 802.11g 64-QAM OFDM modulation. An RF mixer and signal generator were used to extend the frequency range to up to 20GHz. Two link lengths were used for the test, a 50µm MMF patch cord and 100m OM3 fibre. Both the Chalmers and VIS devices were biased at 9mA for this test and the temperature was set to 25°C. The devices were tested at frequencies up to 20GHz. Figure 37 shows the EVM of the VIS device as a function of frequency.

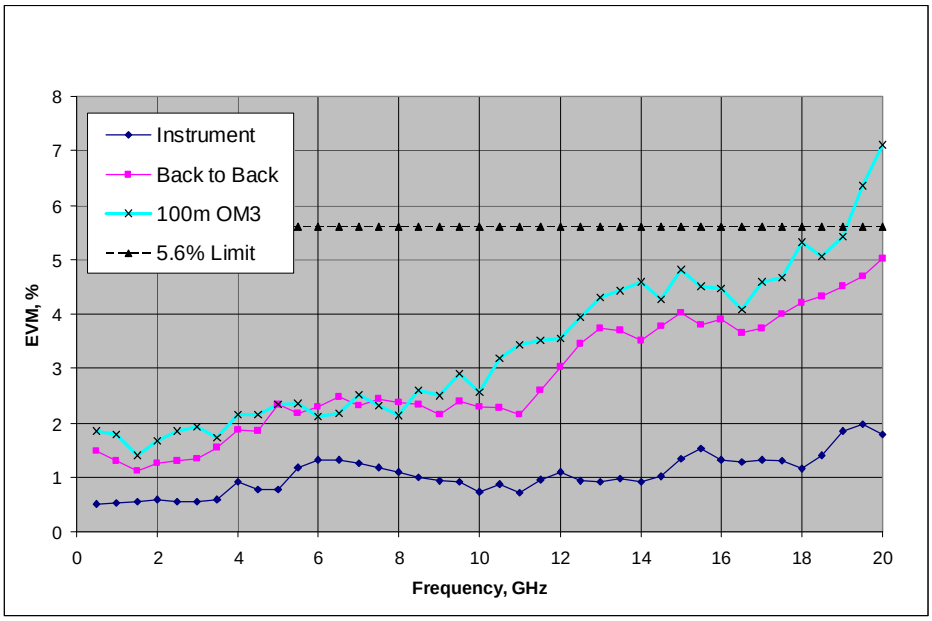


Figure 37 - 28µm mesa diameter VIS VCSEL EVM against frequency

The EVM remained within the 5.6% limit for IEEE 802.11g operation at frequencies up to 20GHz. With an optical link of 100m OM3 fibre, this was reduced to 19GHz. These are the highest carrier frequencies for complex modulation formats achieved with a VCSEL at 850nm. Figure 38 shows the received signal constellation at 16GHz with a 100m OM3 fibre optical link.

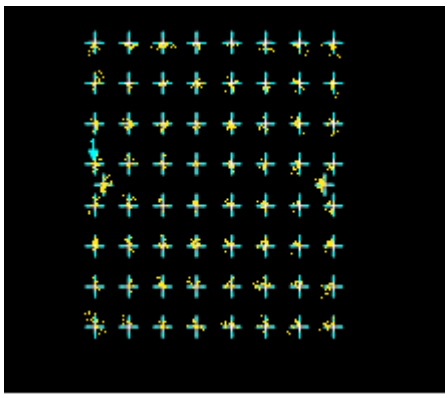


Figure 38 - Received constellation at 16GHz with an optical link of 100m OM3 fibre

Figure 39 shows the EVM of the Chalmers device as a function of frequency. The EVM remained within the 5.6% limit at frequencies up to 15GHz. With an optical link of 100m OM3 fibre, this was reduced to 14.5GHz.

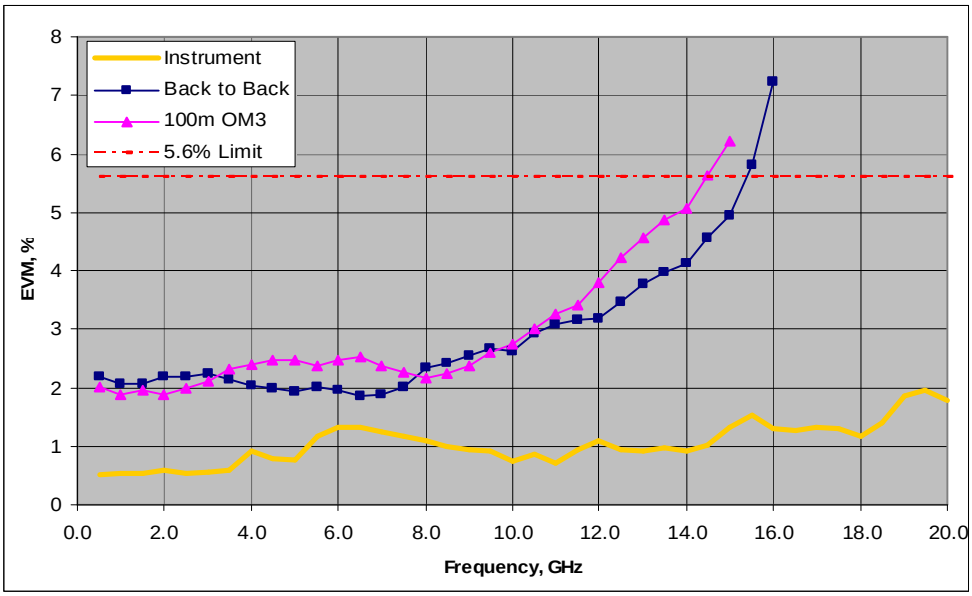


Figure 39 - 13µm oxide aperture Chalmers VCSEL EVM against frequency

The carrier frequencies achieved by both devices show they are suitable for use in RoF applications such as 3G and WLAN services. They are also suitable for use in many upcoming ultra-wideband (UWB) applications which operate at frequencies between 3.1GHz to 10.6GHz such as wireless USB and wireless video distribution. They could also be used in future applications where carrier frequencies up to 20GHz are required.

3.4. Conclusion

- SFDR for 28µm mesa diameter VIS and 13µm oxide aperture Chalmers VCSELs measured under different bias currents and different temperatures.
- EVM measured for both devices using an optical link of 100m OM3 fibre
- Good SFDR performance demonstrated by both devices, with SFDR values remaining above 85dB.$Hz^{2/3}$ at up to 20GHz under high bias currents.
- VIS device demonstrated good EVM performance at frequencies as high as 20GHz, the highest carrier frequencies achieved for a VCSEL operating at 850nm.
- Both devices have shown they are suitable for use in next generation RoF applications.

4. References

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